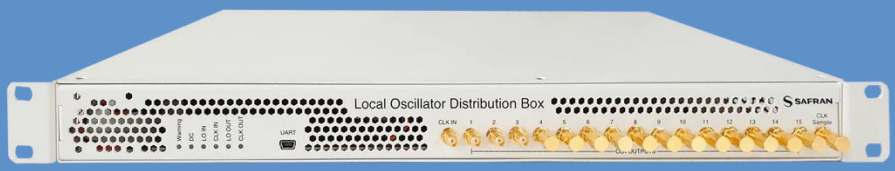
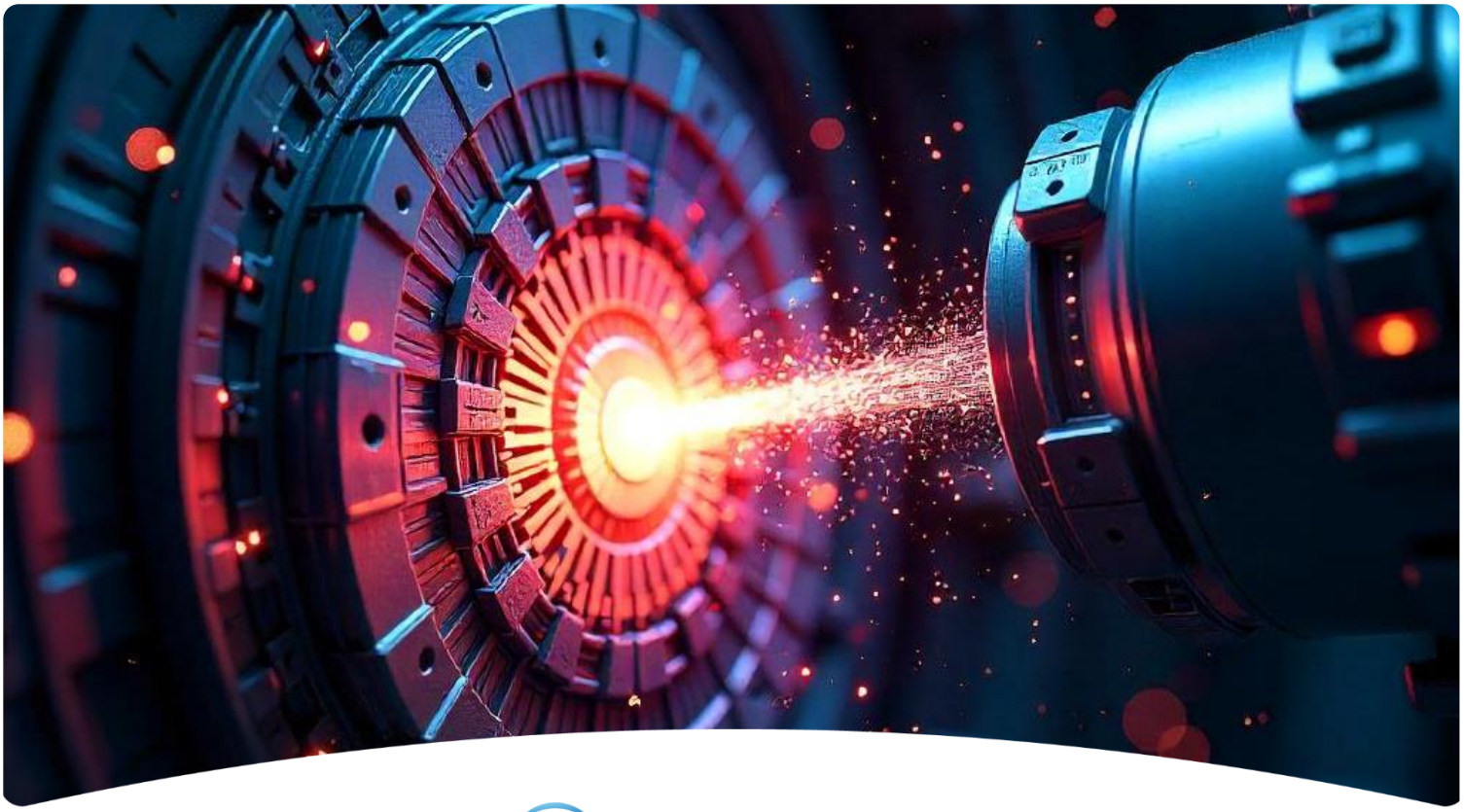
Local Oscillator Distributor (LOD)

Double 1:16 ultra low-noise RF signal splitter



- Number of input clocks: 2 (sinusoidal)
- Maximum input power: +12dBm
- Number of output clocks: 2×16 (sinusoidal)
- Output power: Input power + 5dBm
- Additive phase noise (10 Hz to 1MHz): < 5fs RMS at 380Mz
- Physical dimensions: 19 inch, 1UA rack
- Remote control system: EPICS and friendly user interface



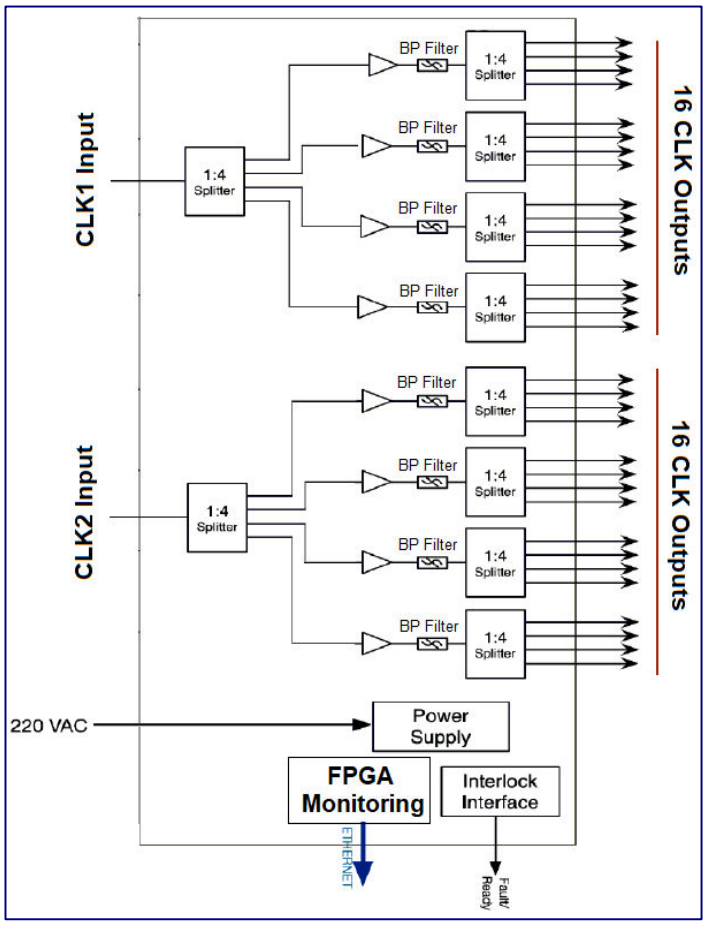
SAFRAN

Local Oscillator Distributor (LOD)

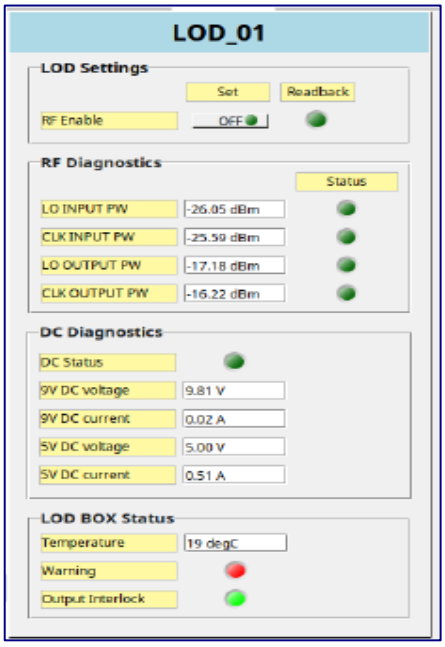
Double 1:16 ultra low-noise RF signal splitter

The "Local Oscillator Distributor" (LOD) is a double 1:16 ultra low-noise RF signal splitter whose main functionality is the distribution of sine clocks with minimal degradation at short distances (tens of meters). For large distance please consider to use the specifically designed timing products.

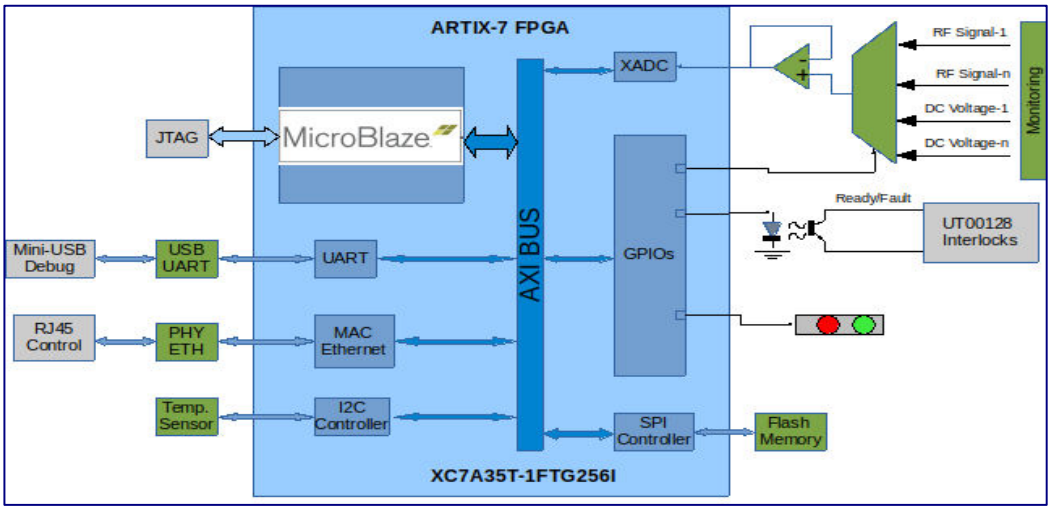
LOD basic block diagram is shown on the next picture.



LOD can be handled through the Ethernet port and the SCPI protocol. This SCPI protocol was released as an additional layer for the IEEE-488.2 standard, used for controlling and monitoring the instruments through GPIB. The FPGA modules scheme and EPICS interface are presented on the next figure.



The system FPGA is dedicated to configure and monitoring the RF signals. An embedded soft-processor is used to provide a simple remote interface to the users.



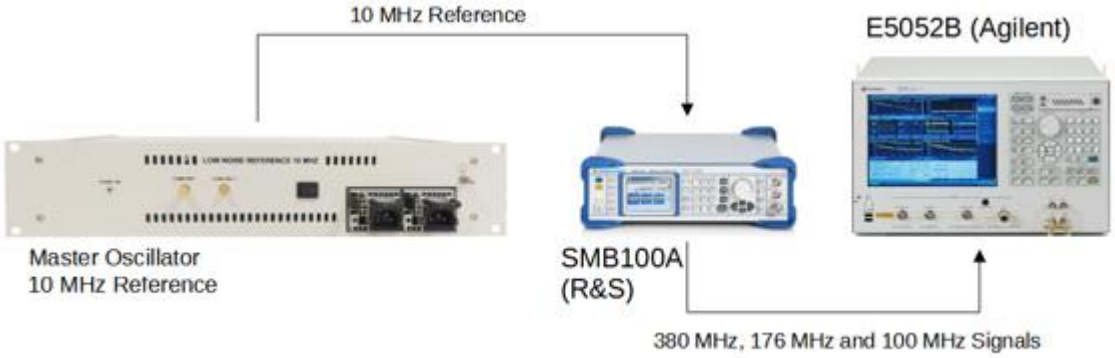
It is complemented with an EPICS driver based on Asyn and StreamDevice module, fully compliant with the EPICS official specifications.

Main characteristics

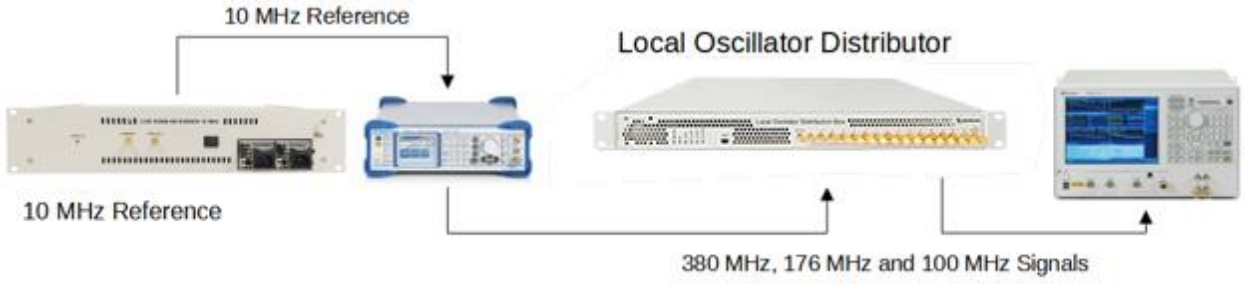
Parameter	Value
Electric features	
Input clocks number	x2 (sinusoidal)
Maximum input power	+12 dBm
Clk output numbers	2x16
Output power level	Input power + 5 dBm
Input Return Loss (S11)	> 14 dB (50Ω)
Harmonics level	< -50dBc
Spurs level	< -70dBc (>1 MHz)
Outputs skew (output phase difference)	< 35 ps (peak-to-peak)
Outputs amplitude unbalance	< 0.5 dB (peak-to-peak)
Additive phase noise (10 Hz to 1 MHz)	< 5 fs rms
Outputs level temperature drift	< 0.05 dB/°C
Power supply	220 VAC, 50 Hz, 30W
Ethernet interface (EPICS monitoring)	1Gbps/100Mbps SCPI
USB interface (debugging)	USB UART (Minicom)
Interlock (Ready/Fault)	Dry contact (normally closed)
Connectors	
RF connectors	SMA female 50Ω
Ethernet connector	RJ45
Interlock connector	Souriau UT00125SH
USB connector	Mini USB
Power connector	IEC C14
Mechanics	
Physical dimensions	19 inchs, 1UA rack
Monitoring	
Internal power voltage (9VDC and 5VDC)	
Internal power current consumption	
Clock1 power input level (level configurable)	
Clock2 power input level (level configurable)	
Clock 1 output #16 power level (level configurable)	
Clock 2 output #16 power level (level configurable)	
Temperature (FPGA internal sensor and I2C external sensor)	
Front panel LEDs	
WARNING (red)	
DC_OK (green)	
CLK1_IN_OK (green)	
CLK2_IN_OK (green)	
CLK1_OUT_OK (green)	
CLK2_OUT_OK (green)	

Examples of results for 380 MHz, 176 MHz and 100 MHz references

The features of the LOD equipment have been validated at different frequencies, in particular, for references at 380 MHz, 176 MHz and 100 MHz (please, consult us the possibility of customizing the equipment to other frequencies). To achieve a precise characterization of the LOD equipment, it is necessary to previously measure the jitter of the reference signal with which the LOD will be fed. For this, a setup like the one indicated in the following figure has been used:



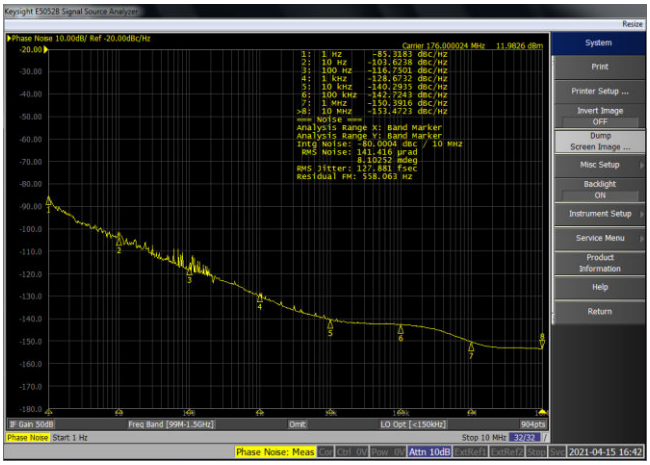
Highlight here the use of the Safran 10 MHz Reference Master Oscillator, essential to ensure that the signal provided by the SMB 100A signal generator maintains low jitter.
Once the phase noise of the input signals to the LOD has been perfectly characterized, a configuration like the next can be used to measure the jitter generated by the equipment:



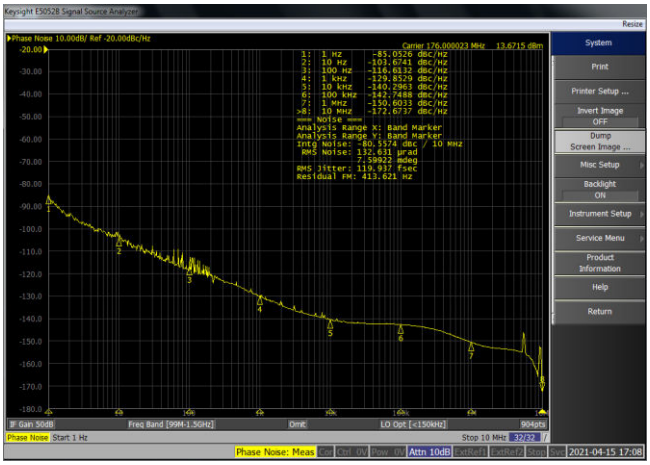
The following figures show on the left the phase noise of the LOD input signals and on the right the measurements of the LOD output phase noise at the frequencies of 380 MHz, 176 MHz and 100 MHz. In all cases the integration range for the jitter is from 1 Hz to 10 MHz. As can be seen, the LOD rms additive jitter is negligible in all cases (< 5 fs rms).

380 MHz reference signal

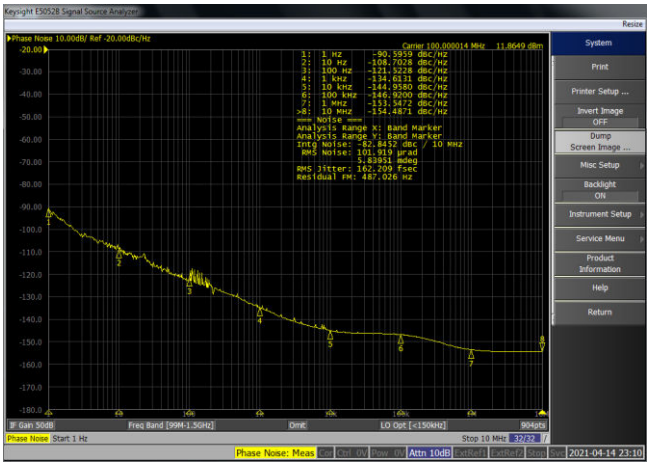
380 MHz LOD output signal



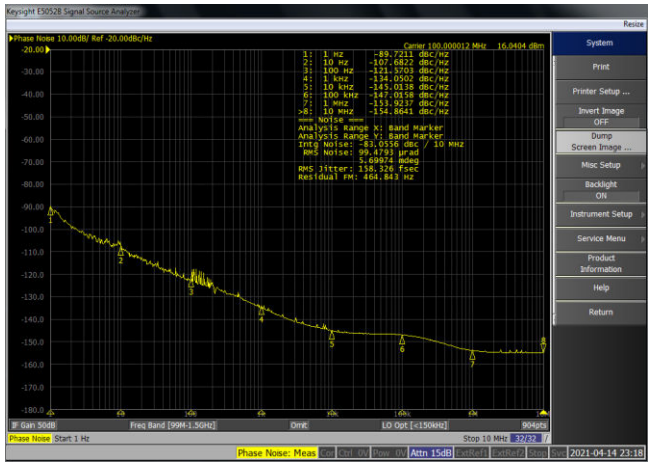
176 MHz reference signal



176 MHz LOD output signal



100 MHz reference signal



100 MHz LOD output signal

POWERED BY TRUST

SAFRAN