TPRO-IP

SYNCHRONIZABLE TIMECODE GENERATOR with IP BUS INTERFACE

User Manual

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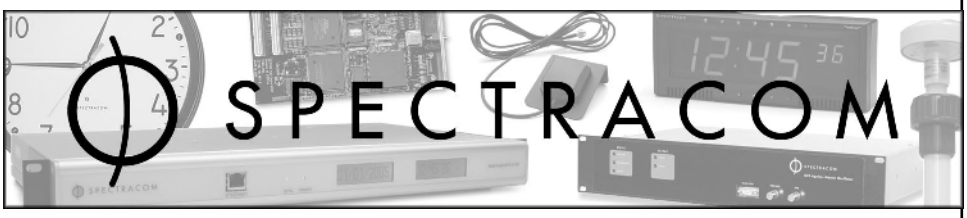

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1 Overview

The TPRO-IP is a precision clock that can be read through a host IP carrier. The TPRO-IP automatically synchronizes to standardized time code signals. It is used for time tagging. Time tagging can be done by reading the clock through four 16-bit time registers or by a logic pulse from the outside world (an "external event"). The 16-bit reads are usually used for software initiated time tagging (for example time-tagging the time a block of data transfer starts or completes). Reading the first 16-bit time register (for units of microseconds through units of milliseconds) also freezes the tens of milliseconds through hundreds of days.

External events are usually used for time-tagging hardware related events (for example the exact time of a radar transmit pulse) because the added error of variation in software delays degrades the accuracy or a software initiated time tag. The time tag data for external events is transferred to the host through a byte wide hardware FIFO as a sequence of 10 bytes.

Inputs to the TPRO-IP are modulated timecode, host commands (not usually needed) and external event pulsed as required for the application.

Outputs are DC level shift IRIG-B time code, and a match pulse that occurs at user commanded times. The TPRO-IP also can generate interrupts to the host system as enabled and selected by the host system. Interrupt sources include external event data FIFO not empty and start or stop time match.

The clock will automatically synchronize to specified time code signals. Status bits advise the host of synchronization status. If there is no synchronization source the TPRO-IP will start counting at 000 days ..00 seconds at power-on. The clock time can be set by user commands.

1.1 Inventory

Before installing the board, please verify that all material ordered has been received. If there is a discrepancy, please contact Spectracom Customer Service at US 585.321.5800.

1.2 Inspection and Support

Unpack the equipment and inspect it for damage. If any equipment has been damaged in transit, please contact Spectracom Customer Service at US 585.321.5800.

If any problems occur during installation and configuration of your Spectracom product, please contact Spectracom Technical Support at US 585.321.5823 or US 585.321.5824.

CAUTION:  *Electronic equipment is sensitive to Electrostatic Discharge (ESD). Observe all ESD precautions and safeguards when handling the timecode generator.*

NOTE: If equipment is returned to Spectracom, it must be shipped in its original packing material. Save all packaging material for this purpose.

NOTE: In this manual, the prefix "0x" indicates that the number is in hexadecimal (Base 16) format.

2 Specifications

2.1 Physical

Dimensions	99.06 mm (3.9”) x 45.72 mm (1.8”) (Industry pack size)
IP bus Type	Single 16-bit
Power	+5V ± 5%, 100mA typical 150 mA max. +12V ± 5%, 100 mA max
Temperature	0 to 50 C operation -40 to 60 C storage
Humidity	0 to 95% non-condensing

2.2 Timecode Input

Code Format	IRIG-B (B122)
Amplitude (mark)	1.2 Vp-p min, 8.0 Vp-p max
Polarity	Detected automatically
Modulation Ratio	2:1 min, 3:1 typ, 4:1 max input
Impedance	> 10 K ohms
Input Time Accuracy	Must be better than 100 ppm

2.3 Timecode Output

Code Format	DC Level Shift IRIG-B (B002)

2.4 Time-Tag Input

Input Voltage	-0.5 V min, +0.8 V max for logic0 +2.0 V min, +5.5 max for logic 1 Tags rising edge
Input Current	<5µA for logic 0 <5µA for logic 1
Rise/Fall Time	500 ns max
Repetition Rate	2000 events per second max timing
Resolution	1 µs

2.5 On-Board Clock

Resolution	1 µs
Range	366:23:59:59.999999
Date Format	Integer (001-366)
Synchronization Time	< 8 seconds

2.6 IP Bus Interface

Meets IP specifications per ANSI/VITA-4 1995	
IP data Transfer cycles supported	
Input/Output (IOSel*)	Eight 16-bit registers
ID Read (IDSEL*)	Identification (12 bytes)
Interrupt	Uses IRQ0 for interrupt at user-specified time

2.7 Match Output

Output Voltage	3.8 V min at 6mA (high) 0.4 V max at –6 mA (low)
Settability	1µs

3 Register Assignments and ID Data

3.1 Register Assignments

Offset from Base Address	Bits Bit 0 is LSB	Read Usage	Write Usage
1		Status	Interrupt Enable
1	7	FIFO not empty interrupt enable	FIFO not empty interrupt enable
	6	MATCH flag interrupt enable	MATCH flag interrupt enable
	5	N/U	N/U
	4	External event enable 1=enable 0=disable set to 0 by reset	External event enable 1=enable 0=disable
	3	MATCH flag	1 = clear flag 0 = no change
	2	In-sync flag 1 = in-sync 0 = non in-sync	Read only
	1	Time code input decodable flag 1 = decodable 0 = not decodable	Read only
	0	FIFO empty flag 0 = empty 1 = not empty	Read only
3	7..0	Data FIFO	Command Port
5	7..0	Interrupt vector	Interrupt vector
9	7..0	N/U	Simulate external event (write any data pattern)
D	7..0	N/U	Reset FIFO and release microcomputer reset
F	7..0	N/U	Assert microcomputer reset
8	15..0 (WORD)	Time (10^3 µS..10^0 µS) Reading this word latches higher order words	N/U
A	15..0 (WORD)	Time (seconds & 100s, 10s or milliseconds)	N/U
C	15..0 (WORD)	Time (hours & minutes)	N/U
E	15..0 (WORD)	Time (days)	N/U

3.2 ID Data

Offset from Base Address	Contents	Comments
81	49	ASCII “I”
83	50	ASCII “P”
85	41	ASCII “A”
87	43	ASCII “C”
89	4F	ID
8B	0	
8D	0	
8F	0	
8F	0	
91	0	
93	0C	ID SIZE
95	CE	CRC

4 Configuration

4.1 Input/output connections

For modulated IRIG-B input operation:

Connect the modulated IRIG-A or IRIG-B source to the IP carrier header pin 1 and the signal ground to pin 2.

Connect the diagnostic LED anode (long lead) to pin 22 and the cathode (short lead) to pin 23.

If using external event input, connect it to pin 9. Else ground pin 9 to pin 10.

Connect pin 31 to pin 32 so IPPS TTL level input doesn't float.

4.2 Base address

The base address of the TPRO-IP in user host space is determined by configuration of the IP carrier and by which slot in the IP carrier the TPRO-IP is placed. For example, the Greenspring Computers VIPC310 VME bus dual IP carrier has a factory default base address of 6000 (for IP slot A) in A16 space.

4.3 Interrupt Request Level

The host bus interrupt level associated with the IRQ0 level signal generated by the TPRO-IP is determined by configuration of the IP carrier. For example, the Greenspring Computers VIPC310 VME bus dual IP carrier has a factory default VME bus IRQ41 for slot A and IRQ2L for slot B.

5 Installation

NOTE: Before installing the TPRO-IP in your system, please make a record of the serial number, the PWB Revision level (example A1 or A, the firmware version labeled on EPROM U3 (example: 4A274A22), and the version labels on FPGA device U5 (example: 4B01A). This information is required for telephone support of the product. Please make the record known to anyone who may require support.

CAUTION:

Observe all ESD procedures when handling the board and the computer. Before installing the board, discharge static buildup by touching the metal frame of the computer with one hand and the protective bag containing the board with the other hand. Open the protective bag only after static buildup has been safely discharged.

Shut down the system.

Install the TPRO-IP board in a IP carrier slot. The TPRO-IP has inputs and outputs that should be connected for the users requirements. There are up to two inputs from the external world: input time code (if used) and a TTL external event pulse (if used). For the TPRO-IP, if input time code is not provided, the board will provide "local" timing starting at 000 days, 00 hours, 00 minutes, 00 seconds. The external event pulses may come from external user equipment, or pulse outputs from the TPRO-IP may be looped back and used as external event inputs with a simple jumper connection. Custom factory configurations will have a manual addendum detailing non-standard I/O configuration.

Start the system.

6 Board Operation

6.1 General

The TPRO-IP operates automatically as soon as the host computer system does the power-on reset. To change the operating parameters or read data consult the Programming section. A status LED can be connected to the 50-pin IP carrier I/O connector for flashing a status pattern to assist in diagnosing installation errors. The pattern is a sequence of short and long flasher. Trailing short flashes are deleted so the status pattern can repeat more frequently.

Flash Position	Meaning of short (cleared) flash	Meaning of long (set) flash
1		Modulated timecode input being used for time reference
2	Synchronization to better than 5μS verified with last 5 seconds	Synchronization to better than 5μS not verified within last 5 seconds
3		In applications with modulated time code inputs only, this status bit will always be set
4		In applications with modulated timecode inputs only, this status bit will always be set
5		In applications with modulated time code inputs only, this status bit will always be set
6	Timecode input being decoded	Timecode input not decodable. In applications without modulated timecode inputs, this status bit will always be set

6.2 Propagation Delay Adjustment

Depending on the actual absolute time accuracy required in the user's application, the TPRO-IP may be commanded to correct for the time required for the time code signal to travel the distance between the time code source and the IP host computer. This delay time is called "propagation delay time" and is about 3.3 microseconds per kilometer for radio time code transmission and about 5 μS per kilometer for copper wire transmission. There is also a time delay on the order of 25 μS that may be caused by small phase shifts due to reactance's at the time code input. To correct for propagation delay, the TPRO-IP can use a propagation delay correction setting ranging between -1000 (because sometime sources transmit early) and +8999 μS. The default setting is 0 μS after the TPRO-IP is reset at power-on or after a RESET command from the user. Users can change the setting by a sequence of programmed commands to the command register on the TPRO-IP. If absolute microsecond accuracy is required, the user will probably need to calibrate the TPRO-IP when it is installed for propagation delay correction by comparing the on-board clock time with a portable reference. The correct propagation delay correction setting is converted on rapidly by trial and error. This setting will not need to be changed unless the location or cabling of the installation is changed. Determining the correct propagation delay setting will probably need the help or a special user program to let various propagation delay settings be tried experimentally while zeroing in on the correct setting. The normal user program should have the capability of using the correct setting once it is determined.

7 Pinouts

7.1 50 Pin IP Carrier Header (P1) Input/Output Pinout

Pin	Signal
1	Ground
2	System Clock 8 MHz
3	Reset Low
4-19	SD0-SD15
20	BS0 Low
21	BS1 Low
22	-12V
23	+12V
24	+5V
25-26	Ground
27	+5V
28	System Read Write Low
29	ID Select
30	Not Used
31	Memory Select
32	Not Used
33	Interrupt Select
34	Not Used
35	Input/Output Select
36	Reserved
37	SA1
38	Not Used
39	SA2
40	Not Used
41	SA3
42	Interrupt Request 0 Low
43	SA4
44	Interrupt Request 1 Low
45	SA5
46	Not Used
47	SA6
48	ACK Low
49	Reserved
50	Ground

7.2 50 Pin IP Carrier Header (P2)

PIN	Signal
1	Modulated timecode input
2	Ground
3	Not used. User should not make connection to these pins.
4,6	Not used. User should not make connection to these pins.
5,7	Not used. User should not make connection to these pins.
8	Not used. User should not make connection to these pins.
9	External event (positive going edge) TTL level input
10	Ground
11	Not used. User should not make connection to these pins.
12	Not used. User should not make connection to these pins.
13	Spare output #1 for future customization
14	Ground
15	Not used. User should not make connection to these pins.
16	Not used. User should not make connection to these pins.
17	Spare output #2 for future customization
18	Ground
19	Not used. User should not make connection to these pins.
20	Ground
21	Not used. User should not make connection to these pins.
22	+5V output for anode side of diagnostic LED. LED must have internal current limiting resistor. **WARNING:** Users should exert extreme care in connections to pin 22. Shorting pin 22 to ground or +12V can damage the TPRO-IP or the host system.
23	Cathode side of diagnostic LED
24	Ground
25	+12V output **WARNING:** Users should exert extreme care in connections to pin 25. Shorting pin 25 to ground or +5V can damage the TPRO-IP or the host system.
26	SPARE3 input for future customization
27	Not used. User should not make connection to these pins.
28,30	Not used. User should not make connection to these pins.
29	Not used. User should not make connection to these pins.
31	Ground side of 47 ohm termination resistor connected to pin 4, 6. Connect to pin 32 to terminate pin 4 or 6 in 47 ohm resistor
32	Ground
33	IRIG-A future customization option. Connects to pin 34 for IRIG-A input
34	IRIG-A future customization option. Connects to pin 33 for IRIG-A input
35,37	Not used. User should not make connection to these pins.
36	Not used. User should not make connection to these pins.
38	IRIG-B DC level shift TTL output
39	MATCH signal TTL level output
40	GATES signal TTL level output
41-50	Microprocessor signal connections for logical analyzer User should make no connections to pins 41-50

8 Programming

User programs interface to hardware and firmware functions of the TPRO-IP. The hardware functions used are:

- Reading the clock through the 16 bit registers
- Reading the status register
- Initializing the data FIFO
- Reading the data FIFO to read external event time tags or command responses
- Enabling/disabling interrupts
- Forcing hardware reset

Firmware functions are initiated by writing 8 bit commands to the command port of the TPRO-IP.

Test programs in the Appendix (Page 36) show examples of these functions.

8.1 Reading the clock through the 16-bit registers

To measure the instantaneous time, a program first does a work I/O read from the low order 16 bit time register at base address + 8 When the low order register is read, the 3 high order time words are stored at the same time in an internal registers in the TPRO-IP. The 3 registers will be frozen until the low order time register is read again. So, whenever the high order registers are read, the time that is returned is the time when the low order register was last read. Any (or none) of the 3 high order registers may be read according to the user's application.

Bits	**15 12**	**11 8**	**7 4**	**3 0**
Data	10^3 µS BCD	10^2 µS BCD	10^1 µS BCD	10^0 µS BCD

Data organization (base address + offset 8)

Bits	**15 12**	**11 8**	**7 4**	**3 0**
Data	10 second BCD	1 second BCD	10^5 µS BCD	10^4 µS BCD

Data organization (base address + offset A)

Bits	**15 12**	**11 8**	**7 4**	**3 0**
Data	10 hour BCD	1 hour BCD	10 minute BCD	1 minute BCD

16-bit word data organization (base address + offset C)

Bits	**15 12**	**11 8**	**7 4**	**3 0**
Data	0	10^2 days BCD	10 day BCD	1 day BCD

Data organization (base address + offset E)

8.2 Status

The meaning of the status bits is defined in the Specifications section of this manual. The Match Interrupt Enable, FIFO Not Empty Interrupt, External Event Enable and Match Flag bits are Read/Write, while all others are read only.

8.3 FIFO Initialization

When a user program starts using the TPRO-IP there may be stale external event or command response data in the FIFO. To initialize the FIFO the user can do a write (any data) to the FIFO Reset port, or the user can just read the FIFO 512 times. Right after initialization, the user should check the FIFO Empty Flag for "0" in case an external event just happened while initializing. Once initialization is done, it does NOT need to be done again so long as the user program makes sure that any data put in the FIFO (in response to external events or user commands) is emptied out by user programs.

8.4 Reading the FIFO

The user program should ALWAYS check the FIFO EMPTY flag (bit 0) for "1" before reading a byte from the FIFO. Otherwise user programs may be reading FIFO data out faster than the TPRO-IP firmware is writing data into the FIFO. Data is always written in 10 byte groups to the FIFO by the TPRO-IP firmware.

8.5 External Event Time Tagging

The External Event Enable bit (Bit 4 in the Status Register) must be a "1" for External Event Time Tags to occur. The enable bit will be cleared by a power on or programmed RESET. Once set to "1" the Enable bit will stay at "1" until written to "0" or a reset occurs.

In response to a rising edge at the external event input (pin 9 on the 50-pin IP header), the TPRO-IP copies the 10 bytes of time data into the on-board FIFO. It takes about 50 µseconds until the last of the 10 bytes is copied into the FIFO. The transfer time fluctuates because the microcomputer may be interrupted while putting data in the FIFO. The time data is accurate to the exact µsecond when the event occurred and the accuracy is not affected by the transfer time.

The occurrence of an external event pulse can be simulated by doing a byte I/O write (any data value) to base address + 3. The simulated external event does not require that the External Event Enable bit in the Status Register be set.

The host program reads captured time information (100s of days through units of µseconds - a total of 10 bytes) sequentially from the FIFO through the TPRO-IP bus interface. Handshaking is done by the host testing the FIFO NOT EMPTY bit (bit 0) of the TPRO-IP status register (base + 1) for "1" *before* each byte is read from the data FIFO (base + 3). The data format for FIFO time stamps is:

Byte	High Nibble	Low Nibble
0	not defined	not defined
1	not defined	defined
2	0	10^2 days
3	10^1 days	10^0 days
4	10^1 hours	10^0hours
5	10^1 minutes	10^0 minutes
6	10^1 seconds	10^0 seconds
7	10^5 µseconds	10^4 µseconds
8	10^3 µseconds	10^2 µseconds
9	10^1 µseconds	10^0µseconds

8.6 Interrupts

The host bus interrupt vector is set by writing to the TPRO-IP base address + 5. The TPRO-IP may be programmed to request interrupts at IRQ0 level upon selectable conditions. Interrupts may be enabled by writing a "1" into the corresponding interrupt enable bit in base address + 1.

Interrupt Condition	Condition Asserted By	User Action to Deassert Condition
FIFO not empty	External event or user command causes on board microprocessor to write data into FIFO	I/O read data from FIFO until FIFO empty or write to FIFO reset port
Match Flag Set	User programmed START or STOP MATCH time is detected	I/O write to base +1 with bit 3 = 1

8.7 Forcing Hardware Reset

The user can reproduce the effect of the host power on reset on the TPRO-IP by writing (any data) to the Assert Microprocessor Reset port (base + F). The RESET will remain asserted until the user writes (any data) to the Reset FIFO port (base + D).

8.8 Commands

Commands are sent as a sequence of bytes to the TPRO-IP command register (base address + 3). All commands should be spaced at least 100 µsec apart so the TPRO-IP firmware has enough time to handle each command. An easy way to generate a processor speed independent 100µsec time delay is to read the TPRO-IP status register 100 times. Without any commands, on cold or warm start the TPRO-IP will automatically synchronize to a modulated time code input. There are commands for:

- Setting time
- Setting propagation delay correction for modulated code input
- Disabling synchronization to input
- Re-enabling synchronization to input
- Simulating power-on reset of TPRO-IP firmware
- Setting MATCH START and MATCH STOP times

Command	Hi Nibble	Lo Nibble
Set time set register 10^3 µS	0	0-9
Set time set register 10^2 µS	1	0-9
Set time set register 10^1 µS	2	0-9
Set time set register 10^0 µS	3	0-9
Set next 1pps time	4	C
Enable resync	4	D
Disable sync	4	E
Reset TPRO-IP firmware	4	F
Set time set register 102 days	5	0-3
Report cog/sog/sats	5	C
Report altitude	5	D
Report longitude	5	E
Report latitude	5	F
Set time set register 10^1 days	6	0-9
Set time set register 10^0 DAYS	7	0-9
Set time set register 10^1 HOURS	8	0-9
Set time set register 10^0 HOURS	9	0-9
Set time set register 10^1 MINUTES	A	0-F
Set time set register 10^0 MINUTES	B	0-F
Set time set register 10^1 SECONDS	C	0-F
Set time set register 10^0 SECONDS	D	0-F
Copy time set register to clock time	E	0
Copy time set register to start/stop hold	E	1
Copy start/stop hold to start match register (days.seconds and time set register (hours,minutes,seconds) to start µS	E	2
Copy start/stop hold to stop match register (days.seconds) and time set register (hours,minutes,seconds) to stop µS	E	3
Clear match flag	E	4
Report firmware ID in FIFO	E	9
Clear set time register	F	0

8.9 Setting Time

The user may set the TPRO-IP for applications where the input reference is not used to be used. If the user does not preset a time, a default preset of 0 days through seconds is used. Setting time will usually be preceded by disabling input synchronization. Otherwise, the TPRO-IP firmware will just switch back from the commanded time to the input time as soon as the input is validated. The sequence of commands for setting time is:

Send CLEAR TIME SET REGISTER command (F0h)
Send SET TIME SET REGISTER commands (5<bcd> through 8<BCD>) for 102 days through 10° seconds in any order
Send COPY TIME SET REGISTER command (E0h)

At least 100 μS should be allowed between sending each command byte. For example to set time to 123 days 01 hours 23 minutes 45 seconds, the sequence F0 51 62 73 80 91 A2 B3 C4 D5 E0 would be sent. As each SET TIME SET REGISTER command is sent, the corresponding digit in an internal time set

buffer in the TPRO-IP will be set. When the COPY TIME SET REGISTER command (E0) is received; the time set buffer will be copied to the clock.

8.10 Setting Propagation Delay Correction

The user may set the compensation for propagation delay between the time code source and the TPRO-IP location. On cold or warm start, the TPRO-IP will assume a propagation delay correction of 0 μS. The sequence of commands for setting propagation delay correction is:

1. Send CLEAR TIME SET REGISTER command (F0h)
2. Send SET TIME SET REGISTER commands (0<bcd> to 3<bcd>)
   For 10^3 μS, 10^2 μS, 10^1 μS, 10°μS, digits in any order
3. Send SET COPY TIME SET REGISTER command (E0h)

Remember to delay at least 100 μS between sending each command byte. For example to set a propagation delay correction value of 1234 μS, the sequence F0 31 22 13 04 E0 would be sent. Some central timing facilities transmit time codes advanced by 1 millisecond. To correct for the advanced time code, it may be desirable to use a negative propagation delay correction setting. Propagation delay settings of 9000 μS to 9999 μS are used to set NEGATIVE propagation delay correction values of -1000 μS to-1μS respectively. For example, to set -500 μS use a setting of 9500 μS. So, the propagation delay correction range of the TPRO-IP is –1000 μS to +8999 μS.

The TPRO-IP can distinguish between COPY TIME SET commands used for setting propagation delay and COPY TIME SET commands used for setting time by noting that different intervening commands have occurred after the CLEAR TIME SET REGISTER command.

8.11 Disabling Synchronization to Input

To prevent the TPRO-IP from synchronizing its time to input signals, send the DISABLE RESYNC (4Eh) command to the TPRO-IP. This is normally used when you set the TPRO-IP time using the Set Generation Time procedure.

8.12 Re-enabling Synchronization to Input

To release the TPRO-IP from a DISABLE RESYNC command, send the ENABLE RESYNC (4Dh) command to the TPRO-IP. The cold or warm start condition for the TPRO-IP is resync enabled.

8.13 Simulating Power-on Reset of TPRO-IP Firmware

The RESET (4Fh) command to the TPRO-IP rests the on-board Z80 microcomputer.

9 Preventive Maintenance & Troubleshooting

9.1 Oscillator Aging Adjustment

NOTE: Applies only to models equipped with -O option ovenized oscillator.

The Oscillator aging adjustment for the TPRO-IP corrects for the effects of aging on the natural crystal oscillator frequency to insure that the undisciplined frequency of the 10 MHz oscillator is 10.000000 MHz ± 10 Hz.

This preventive maintenance should be once every 2 years.

You will need

- A digital frequency counter with 1 PPM or better accuracy and 1 HZ or better resolution (be *sure* that the counter is calibrated)
- A small screwdriver

If you have a custom crystal oscillator in your unit, consult the oscillator data sheet for adjustment method.

Extend the carrier module on which the TPRO-IP is mounted.

Connect a *calibrated* frequency counter to the 10 MHz signal at XO1 pin 8.

Power the system up and wait at least five minutes for the on-board crystal oven temperature to stabilize. Then adjust R10 (using the "solder side" access hole) for 10MHz±10Hz. If R10 is not present, you do not have the -O option and cannot adjust the oscillator.

Power down your system, and reinstall carrier without extender.

9.2 Troubleshooting

9.2.1 Before you contact Spectracom

Have the serial number, Rev level, firmware and FPGA ID you were instructed to record during installation. Please include them in any faxes. Try to exhibit the problem in as reduced (fewest boards in the system) configuration as you can. Try to run our examples, modified as little as possible, to be sure that what you think is a hardware problem is really a software problem.

9.2.2 Bus Crashes

If your program crashes due to a bus error when trying to access the TPRO-IP your problem may be:

Board address configured for IP carrier slot used by TPRO-IP doesn't agree with what your program uses.

9.2.3 Bad data from 16bit data registers

If your program doesn't crash but gets crazy (illegal BCD etc) data from the 16 bit registers your problem may be:

- You are using an address that maps into a different host bus device. To check this hypothesis, remove the TPRO-IP from the IP carrier. If you still can access data from the same address, you are not addressing the TPRO-IP.
- You are using a base address that maps into both the TPRO-IP and another host bus device.
- You are accessing high order bits at base +A, +C, or +E before freezing & reading low order bits at base +8.
- You are reading data (especially if there's lots or zeros) before the TPRO-IP has synchronized to the input code. Remember that there is about a 20-second delay from power on before the TPRO-IP jam syncs to the input code.
- You did a TIME SET command sequence with crazy values

9.2.4 Bad data from FIFO port

If your program doesn't crash, but has crazy (illegal BCD etc) data from the FIFO your problem may be:

- Your code doesn't check the FIFO NOT EMPTY bit in the STATUS REGISTER for "1" *before* reading each byte from the FIFO. If your data contains "00" or seems to slip (hours show up where you expected minute's etc) this is very likely the reason.
- You are reading data (especially if there's lots of zeros) before the TPRO-IP has synchronized to the input code. Remember that here is about a 20-second delay from power on before the TPRO-IP jam syncs to the input code. You did a TIME SET command sequence with crazy values.
- You are using an address that maps into memory or into a different device.

9.2.5 Interrupt crashes

Make sure that the interrupt vector register is correctly initialized.

Make sure that the host bus IRQ level agrees with the configuration of the IP carrier for the slot in which the TPRO-IP is installed.

If you are using the FIFO NOT EMPTY interrupt selection, disable the interrupt enable either at the TPRO-IP or at the host interrupt controller while reading the FIFO or you may caused nested FIFO NOT EMPTY interrupts as each byte is read from the FIFO and the IRQ line toggles.

9.2.6 Board never syncs to input code

If the "in-sync" status bit is "0" (indicating an error):

In-sync *should* be "0" in many cases. A "0" does not mean that there is a fault in the board. Remember that there is about a 20 second delay from power on before the TPRO-IP jam syncs to the input code.

Does the diagnostic LED indicate decodable input signal? If not, the TPRO-IP doesn't see a signal that it can decode. Check signal amplitude and connections.

Examine the input signal on an oscilloscope and make sure that it meets the input specifications of the TPRO-IP.
Is the time code carrier frequency stable to ±100 PPM? Does it make periodic large (larger than 5 μS) time jumps? Tape playback is very likely to have high frequency error unless you use a calibrated servo track to accurately control speed.

9.3 Firmware Sample Code

```
 3                          ********************************************************************************
 4                          * TITLE IPTST1.001 7NOV94 JCK TPRO-IP VME BUS, INTR, COUNTER TESTS
 5                          * FOR THIS DEMO, HOST IS A XYCOM XVME-600 (10 MHZ 68000) + GREENSPRING VIPC310
 6                          ********************************************************************************
 7        00FF 0000         ILLEGAL          EQU    $FF0000
 8        00FF 6001         IPSTS            EQU    $FF6001
 9        0000 0000         BSTSOR           EQU    0          BIT0: FIFO NOT EMPTY    READ ONLY.
10        0000 0001         BSIGOK           EQU    1          BIT1: INPUT TIME CODE DECODEABLE. READ ONLY
11        0000 0002         BSYNCOK          EQU    2          BIT2: GOOD SYNC     READ ONLY
12        0000 0003         BMAT             EQU    3          BIT3: MATCH STATUS. READ ONLY
13        0000 0004         BEXTENB          EQU    4          BIT6: EXTERNAL EVENT ENABLE. READ/WRITE
14        0000 0006         BMATIE           EQU    6          BIT4: MATCH INTERRUPT ENABLE. READ/WRITE
15        0000 0007         BORIE            EQU    7          BIT7: FIFO NOT EMPTY INTR ENABLE. READ/WRITE
16        00FF 6003         IPCMD            EQU    $FF6003     COMMAND PORT (WRITE ONLY)
17        00FF 6003         IPFIFO           EQU    $FF6003     FIFO DATA PORT (READ ONLY)
18        00FF 6005         IPVEC            EQU    $FF6005     INTR VECTOR FOR IRQ0 (READ/WRITE)
19        00FF 6009         IPTAG            EQU    $FF6009     SIMULATED EXTERNAL EVENT PORT. WRITE ONLY
20        00FF 600D         IPFIFR           EQU    $FF600D      FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
21        00FF 600F         IPRESET          EQU    $FF600F     LOCKS TPRO-IP IN RESET. WRITE ONLY
22        00FF 6008         IPLO             EQU    $FF6008      A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
23        00FF 600E         IPHI             EQU    $FF600E      A16 BUS WINDOW FOR MVME133+BASE+E OFFSET
24        00FF 6081         IPID             EQU    $FF6081     ID DATA. SEE IDCHK FOR CORRECT CONTENTS
25  000000  2A7C 0000 0533 START:             MOVEA.L #STRTMSG,A5
26  000006  6100 0390                        BSR    MESSAGE
27                          ********SCAN A16 SPACE FOR DTACKS. TPRO-IP SHOULD BE AT 60XX. AITG MAYBE 0A0X
28  00000A  23CF 0000 03A6                    MOVEA.L A7,SPSAV
29  000010  2038 0008                        MOVE.L  $8,D0
30  000014  7201                             MOVE.L  #1,D1                INCREMENT FOR ADDRESS ON 1ST PASS
31  000016  3801                             MOVE    D1,D4                INIT AITG-VME NOT FOUND
32  000018  3801                             MOVE    D1,D4                 INIT TPRO-IP NOT FOUND
33  00001A  23F8 0008 0000 03AA               MOVE.L  $8,SPSAV+4
34  000022  21FC 0000 006E 0008               MOVEA.L #TRAPISR,$8    ADDRESS OF INTR SERVICE ROUTINE FOR BERR
35  00002A  227C 00FE FFFF                    MOVEA.L #ILLEGAL-1,A1
36  000030  D3C1                    INCNEXT:ADD.L   D1,A1
37  000032  1411                    NEXT:   MOVE.B  (A1),D2
38  000034  3609                            MOVE    A1,D3
39  000036  0243 FF00                        AND     #$FF00,D3
40  00003A  0C43 6000                        CMP.W   #$6000,D3      IF IN TPRO-IP RANGE, WILL=0
41  00003E  6700 0028                        BEQ     DT60XX
42  000042  0C43 A000                        CMP.W   #$A000,D3      IF IN AITGVME RANGE, WILL=0
43  000046  6700 001A                        BEQ     DT0A0X
44  00004A  2A7C 0000 0597                   MOVEA.L #MYSTER,A5
45  000050  6100 0340                        BSR     FATAL
46  000054  2A7C 0000 056E          NO60XX: MOVEA.L #NODTACK,A5
47  00005A  6100 033C                        BSR     MESSAGE
48  00005E  7200                             MOVE.L  #0,D1          PREVENT FURTHER ADDR INCR FOR SCOPE LOOP
49  000060  60D0                             BRA     NEXT
50  000062  383C 0000               DT0A0X: MOVE    #0,D4          FLAG AITG-VME FOUND
51  000066  60C8                             BRA     INCNEXT
52  000068  3A3C 0000               DT60XX: MOVE    #0,D5          FLAG TPRO-IP FOUND
53  00006C  60C2                             BRA     INCNEXT
54  00006E  2E79 0000 03A6          TRAPISR:MOVEA.L SPSAV,A7       POP TRAP ADDR
55  000074  B3FC 00FF FFFF                   CMP.L   #$0FFFFFF,A1   EXHAUSTED A16 SPACE ?
56  00007A  66B4                             BNE     INCNEXT        NO
57  00007C  8A45                             OR      D5,D5          YES - WAS TPRO-IP DTACK FOUND ?
58  00007E  66D4                             BNE     NO60XX         NO
59  000080  21F9 0000 03AA 0008              MOVE.L  SPSAV+4,$8     YES - RESTORE ORIG BERR ISR
```

```
60                                  ************************** CHECK ID DATA **************************
61  000088  2A7C 0000 05C2                  MOVEA.L #IDBEG,A5
62  00008E  6100 0308                       BSR     MESSAGE
63  000092  323C 03E8                       MOVE    #1000,D1        LOOP COUNT FOR 1000 CHECKS OF ID DATA
64  000096  227C 00FF 6081          IDLOP1  MOVEA.L #IPID,A1
65  00009C  247C 0000 041F                  MOVEA.L #IDCHK,A2
66  0000A2  303C 000B                       MOVE    #11,D0          CHECK 12 BYTES
67  0000A6  B509                    IDLOP2  CMP.B   (A1)+,(A2)+
68  0000A8  6600 0010                       BNE     IDBADA
69  0000AC  4A19                            TST.B   (A1)+           TEST ONLY ODD BYTE ADDRESSES
70  0000AE  51C8 FFF6                       DBF     D0,IDLOP2       CHECK 12 BYTES EACH PASS
71  0000B2  51C9 FFE2                       DBF     D1,IDLOP1       DO 1000 PASSES
72  0000B6  6000 0012                       BRA     IE              IF ALL 12 BYTES OK FOR ALL PASSES
73  0000BA  4A21                    IDBADA  TST.B   -(A1)           MOVE ADDRESS BACK TO ERROR ADDRESS
74  0000BC  2A7C 0000 05F4                  MOVEA.L #IDBAD,A5
75  0000C2  6100 02D4                       BSR     MESSAGE
76  0000C6  4A11                    IDBADL  TST.B   (A1)            LOOP ON BAD ADDRESS
77  0000C8  60FC                            BRA     IDBADL
78                                  ************************** TEST IE BITS CAN BE SET **************************
79  0000CA  2A7C 0000 0624              IE  MOVEA.L #IETST,A5
80  0000D0  6100 02C6                       BSR     MESSAGE
81  0000D4  13FC 00C0 00FF 6001             MOVE.B  #(1.SHL.BORIE)+(1.SHL.BMATIE),IPSTS
82  0000DC  1039 00FF 6001                  MOVE.B  IPSTS,D0
83  0000E2  0200 00C0                       ANDI.B  #(1.SHL.BORIE)+(1.SHL.BMATIE),D0
84  0000E6  0C00 00C0                       CMPI.B  #(1.SHL.BORIE)+(1.SHL.BMATIE),D0
85  0000EA  6700 000C                       BEQ     IESETOK
86  0000EE  2A7C 0000 065A                  MOVEA.L #IENOSET,A5
87  0000F4  6100 02A2                       BSR     MESSAGE
88                                  ************************** TEST RESET CLEARS IE BITS **************************
89  0000F8  2A7C 0000 0681      IESETOK MOVEA.L #RSTTST,A5
90  0000FE  6100 0298                       BSR     MESSAGE
91  000102  13C0 00FF 600F                  MOVE.B  D0,IPRESET
92  000108  0839 0006 00FF 6001             BTST.B  #BMATIE,IPSTS
93  000110  6700 000C                       BEQ     FIFO
94  000114  2A7C 0000 06BA                  MOVEA.L #RSTBAD,A5
95  00011A  6100 0276                       BSR     FATAL
96  00011E  2A7C 0000 06EE          FIFO    MOVEA.L #FIFTST,A5
97  000124  6100 0272                       BSR     MESSAGE
98  000128  13C1 00FF 600D                  MOVE.B  D1,IPFIFR       PURGE FIFO
99  00012E  0839 0000 00FF 6001             BTST.B  #BSTSOR,IPSTS   MAKE SURE FIFOOR=0 AFTER PURGE
100 000136  6700 0002                       BEQ     ECHTST
101                                 ********COMMAND TPRO-IP INTO ECHO MODE & ECHO 1B-FF, 01-1A 100 TIMES ********
102 00013A  2A7C 0000 077C      ECHTST  MOVEA.L #ECHOBEG,A5
103 000140  6100 0256                       BSR     MESSAGE
104 000144  13FC 001B 00FF 6003             MOVE.B #$1B,IPCMD       PUT TPRO-IP IN ECHO MODE
105 00014C  303C 07D0                       MOVE    #2000,D0
106 000150  6100 01D2                       BSR     WT100L          WAIT FOR "1B" TO ECHO
107 000154  4A39 00FF 6003                  TST.B   IPFIFO          PURGE 1B
108 00015A  343C 0014                       MOVE    #20,D2          DO 20 LOOPS OF ALL VALUES
109 00015E  123C 0000           ECHOTOP:MOVE.B  #0,D1
110 000162  0601 0001            CMDLOP: ADDI.B  #1,D1
111 000166  6700 000E                       BEQ     WTECHOL         IF 1-255 WRITTEN TO CMD PORT
112 00016A  6100 01B4                       BSR     WT100
113 00016E  13C1 00FF 6003                  MOVE.B  D1,IPCMD
114 000174  60EC                            BRA     CMDLOP
115 000176  0601 0001           WTECHOL:ADDI.B  #1,D1
116 00017A  6700 002E                       BEQ     ECHLOP2
```

```
117  00017E  0839 0000 00FF 6001          BTST.B  #0,IPSTS      BYTE SHOULD BE ECHOED TO FIFO NOW
118  000186  6700 0016                    BEQ     NOECHER       IF NOT, REPORT NO ECHO & TRY AGAIN
119  00018A  1639 00FF 6003               MOVE.B  IPFIFO,D3     COMPARE ECHOED BYTE WITH ORIGINAL
120  000190  B203                         CMP.B   D3,D1
121  000192  67E2                         BEQ     WTECHOL
122  000194  2A7C 0000 07BE     BADECH    MOVEA.L #ECHOBAD,A5
123  00019A  6100 01F6                    BSR     FATAL
124  00019E  2A7C 0000 07F2     NOECHER:  MOVEA.L #NOECHO,A5
125  0001A4  6100 01F2                    BSR     MESSAGE
126  0001A8  60FE                 HERE    BRA     HERE
127  0001AA  51CA FFB6          ECHLOP2   DBF     D2,CMDLOP      DO ALL 255 VALUES 100 TIMES
128  0001AE  13C1 00FF 6003               MOVE.B  D1,IPCMD       REMOVE FROM ECHO MODE. 00 BYTE WILL ECHO
129  0001B4  6100 016A                    BSR     WT100
130  0001B8  1039 00FF 6003               MOVE.B  IPFIFO,D0      CLEAR OUT 00 BYTE FROM FIFO
131  0001BE  2A7C 0000 082E               MOVEA.L #ECHOOK,A5
132  0001C4  6100 01D2                    BSR     MESSAGE
133  0001C8  323C 0000                    MOVE    #0,D1          TRY 0-255 VECTOR PATTERN
134  0001CC  13C1 00FF 6005      VECLOP   MOVE.B  D1,IPVEC       WRITE TO INT VECTOR REG
135  0001D2  B239 00FF 6005               CMP.B   IPVEC,D1
136  0001D8  6600 0012                    BNE     BADVECT
137  0001DC  0601 0001                    ADDI.B  #1,D1          ALL DONE ?
138  0001E0  66EA                         BNE     VECLOP         NO
139  0001E2  2A7C 0000 0891               MOVEA.L #VECOK,A5
140  0001E8  6000 0008                    BRA     INT0TST
141  0001EC  2A7C 0000 0868     BADVECT   MOVEA.L #VECERR,A5     REPORT BAD VECTOR ECHO
142                                      ********CHECK THAT 1PPS, NOSYNC, INSYNC AND FIFO INTERRUPTS WORK OK
143  0001F2  6100 01A4          INT0TST   BSR     MESSAGE
144  0001F6  21FC 0000 0382 0100          MOVEA.L #INT0ISR,$100
145  0001FE  3A3C 0019                    MOVE    #$19,D5        INIT INTR PRIORITY TO 1
146  000202  383C 2000                    MOVE    #$2000,D4      SET STS LEV = TO ALLOW INTR1
147  000206  13FC 0040 00FF 6005          MOVE.B  #$40,IPVEC
148  00020E  46C4                         MOVE    D4,SR          SET STS LEV = TO ALLOW INTRX
149  000210  13FC 0000 0000 03AE          MOVE.B  #0,SPSAV+8     INIT INTR COUNTS
150  000218  13FC 0000 00FF 6009          MOVE.B  #0,IPTAG       FORCE EVENT DATA INTERRUPT
151  000220  13FC 0080 00FF 6001          MOVE.B  #$80,IPSTS     ENABLE FIFO RDY INTR
152  000228  6100 00F6                    BSR     WT100          WAIT FOR EVENT INTR
153  00022C  2A7C 0000 094B               MOVEA.L #INTROK,A5     REPORT IRQ0 OK AT CURRENT L,A6
154  000232  0C39 0000 0000 03AE          CMPI.B  #0,SPSAV+8     EVENT INTR OK ?
155  00023A  6600 0008                    BNE     IRQRPT         YES
156  00023E  2A7C 0000 091F               MOVEA.L #NOEVTI,A5     REPORT MISSING EVENT INTR.
157  000244  6100 0152           IRQRPT   BSR     MESSAGE
158                                      ********CHECK SECONDS 0-59 PARALLEL=FIFO TIME********
159  000248  13C0 00FF 600D      CHKSEC   MOVE.B  D0,IPFIFR      CLEAR FIFO OF IRQ0 TEST DATA
160  00024E  6100 00E2                    BSR     TAGNPAR        GET TIME TAG FIFO DATA & PARALLEL TIME
161  000252  207C 0000 03BA               MOVEA.L #HISAV+8,A0
162  000258  247C 0000 03C2               MOVEA.L #DELTA+8,A2
163  00025E  023C 0000                    ANDI.B  #0,CCR
164  000262  1520                         MOVE.B  -(A0),-(A2)    DELTA = PARALLEL - FIFO
165  000264  4A1A                         TST.B   (A2)+          SBCD NEEDS AUTODEC MODE
166  000266  8509                         SBCD    -(A1),-(A2)
167  000268  323C 0006                    MOVE    #6,D1          DO 7 MORE BYTES
168  00026C  1520                DELTLOP  MOVE.B  -(A0),-(A2)    DELTA = PARALLEL - FIFO
169  00026E  4A1A                         TST.B   (A2)+          SBCD NEEDS AUTODEC MODE
170  000270  4200                         CLR.B   D0             SET Z
171  000272  8509                         SBCD    -(A1),-(A2)
172  000274  6600 003E                    BNE     NONZERO        ** REPLACE WITH NO-OP FOR WW PROTO **
173  000278  51C9 FFF2                    DBF     D1,DELTLOP
```

```
174  00027C  1039 0000 0431                  MOVE.B  EVTDAT+6,D0
175  000282  B039 0000 041E                  CMP.B   SECSAV,D0       SECONDS CHANGE  ?
176  000288  67BE                            BEQ     CHKSEC
177  00028A  13F9 0000 0431 0000             MOVE.B  EVTDAT+6,SECSAV
                041E
178  000294  2A7C 0000 097B                  MOVEA.L #TICMSG,A5      YES - WRITE A TIC
179  00029A  6100 00FC                       BSR     MESSAGE
180  00029E  4A39 0000 0430                  TST.B   EVTDAT+5        MINUTES NON-ZERO ?
181  0002A4  67A2                            BEQ     CHKSEC          NO - KEEP GOING
182  0002A6  2A7C 0000 08B1                  MOVEA.L #DELTOK,A5
183  0002AC  6100 00EA                       BSR     MESSAGE
184  0002B0  6000 000C                       BRA     CHKMD           YES - CHECK MINUTES..DAYS
185  0002B4  2A7C 0000 08EE   NONZERO MOVEA.L #DELTBAD,A5
186  0002BA  6100 00D6                       BSR     FATAL
187                          ******************************************************
188  0002BE  207C 0000 0435     CHKMD   MOVEA.L #TIMSET,A0
189  0002C4  227C 0000 03C2             MOVEA.L #TIMCHK,A1
190  0002CA  6100 0042          CHKMDL  BSR     CMDSTR          SEND TIME SET COMMANDS
191  0002CE  303C 0FFF                  MOVE    #$FFF,D0
192  0002D2  6100 0050                  BSR     WT100L          WAIT FOR TIME SET
193  0002D6  4A79 00FF 6008             TST     IPLO            LATCH TIME
194  0002DC  2A7C 0000 09B3             MOVEA.L #DDDMSG,A5
195  0002E2  3039 00FF 600E             MOVE    IPHI,D0
196  0002E8  B059                       CMP     (A1)+,D0        0DDD OK ?
197  0002EA  6600 00A6                  BNE     FATAL           NO
198  0002EE  2A7C 0000 097D             MOVEA.L #HHMMMSG,A5
199  0002F4  3039 00FF 600C             MOVE    IPLO+4,D0       HHMM
200  0002FA  B059                       CMP     (A1)+,D0        HR..MIN OK ?
201  0002FC  6600 0094                  BNE     FATAL           NO
202  000300  4A10                       TST.B   (A0)            DONE WITH CHKMD TEST ?
203  000302  66C6                       BNE     CHKMDL
204  000304  2A7C 0000 09E9     MDDON   MOVEA.L #CHKMDOK,A5
205  00030A  6000 0086                  BRA     FATAL
206  00030E  1018                CMDSTR: MOVE.B  (A0)+,D0        SEND NON-0 COMMANDS (A0) SPACED BY WT100
207  000310  6700 001E                  BEQ     WTRTS
208  000314  13C0 00FF 6003             MOVE.B  D0,IPCMD
209  00031A  6100 0004                  BSR     WT100
210  00031E  60EE                       BRA     CMDSTR
211  000320  303C 00FF            WT100:  MOVE    #$FF,D0
212  000324  0839 0001 00FF 6001 WT100L: BTST.B  #1,IPSTS        LIMITS LOOP SPEED TO I/O SPEED
213  00032C  51C8 FFF6                  DBF     D0,WT100L
214  000330  4E75                WTRTS:  RTS
215                                      ******** SUBROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6 *****
216  000332  13FC 0000 00FF 6009 TAGNPAR MOVE.B  #0,IPTAG        TRIGGER EVENT BCD TIME REPORT
217  00033A  33F9 00FF 6008 0000        MOVE    IPLO,HISAV+6
           03B8
218  000344  33F9 00FF 600A 0000        MOVE    IPLO+2,HISAV+4
           03B6
219  00034E  33F9 00FF 600C 0000        MOVE    IPLO+4,HISAV+2
           03B4
220  000358  33F9 00FF 600E 0000        MOVE    IPHI,HISAV
           03B2
221  000362  227C 0000 042B             MOVEA.L #EVTDAT,A1
222  000368  323C 0009                  MOVE    #9,D1
223  00036C  0839 0000 00FF 6001 WTFIFA: BTST.B  #0,IPSTS      READ 10 BYTES OF FIFO DATA
224  000374  67F6                       BEQ     WTFIFA
225  000376  12F9 00FF 6003             MOVE.B  IPFIFO,(A1)+  READ WITHOUT MESSING UP A REGISTER
```

```
226  00037C  51C9 FFEE                    DBF    D1,WTFIFA
227  000380  4E75                         RTS
228  000382  5239 0000 03AE         INT0ISR:ADD.B  #1,SPSAV+8   TELL BACKGROUND CODE THAT INTR HAPPENED
229  000388  13FC 0000 00FF 6001          MOVE.B #0,IPSTS     DISABLE FIFO OR INTR
230  000390  4E73                         RTE
231  000392  6100 0004               FATAL: BSR    MESSAGE       FATAL ERROR REPORT
232  000396  60FE                  FATALW BRA    FATALW
233  000398  3C4D                  MESSAGE:MOVE   A5,A6
234  00039A  4A1E                  MSGEND: TST.B  (A6)+       FIND END OF MESSAGE
235  00039C  66FC                         BNE    MSGEND
236  00039E  4A26                         TST.B  -(A6)
237  0003A0  4E4F                         TRAP   #15
238  0003A2  0006                         DW     $6          DISPLAY STRING. NO AUTO CR/LF
239  0003A4  4E75                         RTS
240  0003A6  0000 0000 0000 0000     SPSAV: LWORD  0,0,0 SPSAV,+4=$8 SAV,+8=INTCNT3..0
          0000 0000
241  0003B2  0000 0000 0000 0000     HISAV: LWORD  0,0  SEC,FRAC
242  0003BA  0000 0000 0000 0000    DELTA: LWORD  0,0
243  0003C2  0000 0001 0000 0002 TIMCHK: WORD   $0000,$0001,$0000,$0002,$0000,$0004,$0000,$0008
          0000 0004 0000 0008
244  0003D2  0000 0010 0000 0020          WORD   $0000,$0010,$0000,$0020,$0000,$0040  * 1 MIN..40 MIN
          0000 0040
245  0003DE  0000 0100 0000 0200          WORD   $0000,$0100,$0000,$0200,$0000,$0400,$0000,$0800
          0000 0400 0000 0800
246  0003EE  0000 1000 0000 2000          WORD   $0000,$1000,$0000,$2000          * 1 HR .. 20 HR
247  0003F6  0001 0000 0002 0000          WORD   $0001,$0000,$0002,$0000,$0004,$0000,$0008,$0000
          0004 0000 0008 0000
248  000406  0010 0000 0020 0000          WORD   $0010,$0000,$0020,$0000,$0040,$0000,$0080,$0000
          0040 0000 0080 0000
249  000416  0100 0000 0200 0000          WORD   $0100,$0000,$0200,$0000          * 1 DAY..200DAY
250  00041E  00                    SECSAV: .BYTE  0
251  00041F  49 50 41 43 4F 00     IDCHK:  .BYTE  "IPAC",$4F,0,0,0,0,0,$0C,$CE
252  00042B  00 00 00 00 00 00     EVTDAT:.BYTE   0,0,0,0,0,0,0,0,0,0
253  000435  50 60 70 80 90 A0     TIMSET:.BYTE   $50,$60,$70,$80,$90,$A0,$B1,$C0,$D0,$E0,0 000:00:01:00
254  000440  50 60 70 80 90 A0              .BYTE  $50,$60,$70,$80,$90,$A0,$B2,$C0,$D0,$E0,0 000:00:02:00
255  00044B  50 60 70 80 90 A0              .BYTE  $50,$60,$70,$80,$90,$A0,$B4,$C0,$D0,$E0,0 000:00:04:00
256  000456  50 60 70 80 90 A0              .BYTE  $50,$60,$70,$80,$90,$A0,$B8,$C0,$D0,$E0,0 000:00:08:00
257  000461  50 60 70 80 90 A1              .BYTE  $50,$60,$70,$80,$90,$A1,$B0,$C0,$D0,$E0,0 000:00:10:00
258  00046C  50 60 70 80 90 A2              .BYTE  $50,$60,$70,$80,$90,$A2,$B0,$C0,$D0,$E0,0 000:00:20:00
259  000477  50 60 70 80 90 A4              .BYTE  $50,$60,$70,$80,$90,$A4,$B0,$C0,$D0,$E0,0 000:00:40:00
260  000482  50 60 70 80 91 A0              .BYTE  $50,$60,$70,$80,$91,$A0,$B0,$C0,$D0,$E0,0 000:01:00:00
261  00048D  50 60 70 80 92 A0              .BYTE  $50,$60,$70,$80,$92,$A0,$B0,$C0,$D0,$E0,0 000:02:00:00
262  000498  50 60 70 80 94 A0              .BYTE  $50,$60,$70,$80,$94,$A0,$B0,$C0,$D0,$E0,0 000:04:00:00
263  0004A3  50 60 70 80 98 A0              .BYTE  $50,$60,$70,$80,$98,$A0,$B0,$C0,$D0,$E0,0 000:08:00:00
264  0004AE  50 60 70 81 90 A0              .BYTE  $50,$60,$70,$81,$90,$A0,$B0,$C0,$D0,$E0,0 000:10:00:00
265  0004B9  50 60 70 82 90 A0              .BYTE  $50,$60,$70,$82,$90,$A0,$B0,$C0,$D0,$E0,0 000:20:00:00
266  0004C4  50 60 71 80 90 A0              .BYTE  $50,$60,$71,$80,$90,$A0,$B0,$C0,$D0,$E0,0 001:00:00:00
267  0004CF  50 60 72 80 90 A0              .BYTE  $50,$60,$72,$80,$90,$A0,$B0,$C0,$D0,$E0,0 002:00:00:00
268  0004DA  50 60 74 80 90 A0              .BYTE  $50,$60,$74,$80,$90,$A0,$B0,$C0,$D0,$E0,0 004:00:00:00
269  0004E5  50 60 78 80 90 A0              .BYTE  $50,$60,$78,$80,$90,$A0,$B0,$C0,$D0,$E0,0 008:00:00:00
270  0004F0  50 61 70 80 90 A0              .BYTE  $50,$61,$70,$80,$90,$A0,$B0,$C0,$D0,$E0,0 010:00:00:00
271  0004FB  50 62 70 80 90 A0              .BYTE  $50,$62,$70,$80,$90,$A0,$B0,$C0,$D0,$E0,0 020:00:00:00
272  000506  50 64 70 80 90 A0              .BYTE  $50,$64,$70,$80,$90,$A0,$B0,$C0,$D0,$E0,0 040:00:00:00
273  000511  50 68 70 80 90 A0              .BYTE  $50,$68,$70,$80,$90,$A0,$B0,$C0,$D0,$E0,0 080:00:00:00
274  00051C  51 60 70 80 90 A0              .BYTE  $51,$60,$70,$80,$90,$A0,$B0,$C0,$D0,$E0,0 100:00:00:00
275  000527  52 60 70 80 90 A0              .BYTE  $52,$60,$70,$80,$90,$A0,$B0,$C0,$D0,$E0,0 200:00:00:00
276  000532  00                           .BYTE  0
```

```
277  000533  4E 4F 57 20 53 45     STRTMSG:ASCII  NOW SEACHING ALL A16 SPACE FOR DTACKS. DISCONNECT INPUT!
278  00056B  0D 0A 00                      .BYTE  $0D,$0A,0
279  00056E  45 52 52 3A 4E 4F   NODTACK:ASCII  ERR:NO TPRO-IP DTACK IN ALL A16 SPACE.
280  000594  0D 0A 00                      .BYTE  $0D,$0A,0
281  000597  45 52 52 3A 57 52          MYSTER: ASCII  ERR:WRONG ADDR A16 DTACK (AT ABORT (A1))
282  0005BF  0D 0A 00                      .BYTE  $0D,$0A,0
283  0005C2  4F 4B 3A 20 46 4F          IDBEG:  ASCII  OK: FOUND TPRO-IP AT 60XX. NOW STARTING ID TEST
284  0005F1  0D 0A 00                      .BYTE  $0D,$0A,0
285  0005F4  45 52 52 3A 49 4E          IDBAD:  ASCII  ERR:INCORRECT ID DATA. REPEATING (A1) FOREVER
286  000621  0D 0A 00                      .BYTE  $0D,$0A,0
287  000624  4F 4B 3A 20 31 30          IETST:  ASCII  OK: 1000 CHECKS OF ID DATA OK. NOW STARTING IE TEST
288  000657  0D 0A 00                      .BYTE  $0D,$0A,0
289  00065A  45 52 52 3A 43 41          IENOSET:ASCII  ERR:CANT SET MATIE AND ORIE IN IPSTS
290  00067E  0D 0A 00                      .BYTE  $0D,$0A,0
291  000681  4F 4B 3A 20 42 4F          RSTTST: ASCII  OK: BOTH IE BITS SET BY WRITE. NOW STARTING RESET TEST
292  0006B7  0D 0A 00                      .BYTE  $0D,$0A,0
293  0006BA  45 52 52 3A 57 52          RSTBAD: ASCII  ERR:WRITE TO RESET DOESNT CLEAR MATCH IE OR OR IE
294  0006EB  0D 0A 00                      .BYTE  $0D,$0A,0
295  0006EE  4F 4B 3A 20 49 50          FIFTST: ASCII  OK: IPSTS RESET & RELEASE OK. NOW TESTING FIFO
296  00071C  0D 0A 00                      .BYTE  $0D,$0A,0
297  00071F  45 52 52 3A 57 52          FIFSBAD:ASCII  ERR:WRITE TO INTERNAL EVT ADDR DOESNT SET FIFOOR
298  00074F  0D 0A 00                      .BYTE  $0D,$0A,0
299  000752  45 52 52 3A 57 52          FIFRBAD:ASCII  ERR:WRITE TO IPFIFR DOESNT CLEAR FIFOOR
300  000779  0D 0A 00                      .BYTE  $0D,$0A,0
301  00077C  4F 4B 3A 20 49 4E          ECHOBEG:ASCII  OK: INT EVT SETS OR, IPFIFR WRT CLRS OR. CMD ECHO TEST STARTING
302  0007BB  0D 0A 00                      .BYTE  $0D,$0A,0
303  0007BE  45 52 52 3A 49 4E          ECHOBAD:ASCII  ERR:INCORRECT CMD DATA ECHO. REPEATING D1 FOREVER
304  0007EF  0D 0A 00                      .BYTE  $0D,$0A,0
305  0007F2  45 52 52 3A 43 4D          NOECHO: ASCII  ERR:CMD DATA (ABORT D1) NOT ECHOED. REPEATING D1 FOREVER.
306  00082B  0D 0A 00                      .BYTE  $0D,$0A,0
307  00082E  4F 4B 3A 20 32 35          ECHOOK: ASCII  OK: 255 COMMANDS ECHOED 20 TIMES EACH. CHECKING VEC REG
308  000865  0D 0A 00                      .BYTE  $0D,$0A,0
309  000868  45 52 52 3A 56 45          VECERR: ASCII  ERR:VECTOR REG DID NOT ECHO (ABORT D1)
310  00088E  0D 0A 00                      .BYTE  $0D,$0A,0
311  000891  4F 4B 3A 20 56 45          VECOK:  ASCII  OK: VECTOR REG WR/RD 0-255 OK
312  0008AE  0D 0A 00                      .BYTE  $0D,$0A,0
313  0008B1  0D 0A              DELTOK: .BYTE  $0D,$0A
314  0008B3  4F 4B 3A 20 50 41          ASCII  OK: PARALLEL TIME - FIFO TAG TIME OK. NOW TEST MIN..DAYS
315  0008EB  0D 0A 00                      .BYTE  $0D,$0A,0
316  0008EE  0D 0A              DELTBAD:BYTE  $0D,$0A
317  0008F0  45 52 52 3A 20 50          ASCII  ERR: PARALLEL TIME - FIFO DIFFERENCE TOO BIG
318  00091C  0D 0A 00                      .BYTE  $0D,$0A,0
319  00091F  45 52 52 3A 4E 4F          NOEVTI: ASCII  ERR:NO IRQ0 INTERRUPT FROM SIM. EXT EVENT
320  000948  0D 0A 00                      .BYTE  $0D,$0A,0
321  00094B  4F 4B 3A 20 49 52          INTROK: ASCII  OK: IRQ0 OK. NOW CHECK USEC..40S OF SECS BITS
322  000978  0D 0A 00                      .BYTE  $0D,$0A,0
323  00097B  59                 TICMSG: ASCII  Y
324  00097C  00                         .BYTE  0
325  00097D  45 52 52 3A 20 48          HHMMMSG:ASCII  ERR: HHMM READ FROM TPRO-IP DOESN'T MATCH SET VALUE
326  0009B0  0D 0A 00                      .BYTE  $0D,$0A,0
327  0009B3  45 52 52 3A 20 30          DDDMSG: ASCII  ERR: 0DDD READ FROM TPRO-IP DOESN'T MATCH SET VALUE
328  0009E6  0D 0A 00                      .BYTE  $0D,$0A,0
329  0009E9  49 50 54 53 54 31          CHKMDOK:ASCII  IPTST1 COMPLETED
330  0009F9  0D 0A 00                      .BYTE  $0D,$0A,0
331  0009FC                             END


      Lines Assembled :  331          Assembly Errors :  0
```

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 3                                  ********************************************************************************
 4                                  * TITLE IPTST2.001 7NOV94 JCK TPRO-IP VME BUS LATCHED VS FIFO DELTA
 5                                  * NOTE: FOR THIS DEMO, HOST IS A XYCOM XVME-600 (10 MHZ 68000)
 6                                  ********************************************************************************
 7                 00FF 6001        IPSTS               EQU    $FF6001
 8                 0000 0000        BSTSOR              EQU    0          BIT0: FIFO NOT EMPTY    READ ONLY.
 9                 00FF 6003        IPFIFO              EQU    $FF6003     FIFO DATA PORT (READ ONLY)
10                 00FF 6009        IPTAG               EQU    $FF6009     SIMULATED EXTERNAL EVENT PORT. WRITE ONLY
11                 00FF 600D        IPFIFR              EQU    $FF600D     FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
12                 00FF 6008        IPLO                EQU    $FF6008     A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
13                 00FF 600E        IPHI                EQU    $FF600E     A16 BUS WINDOW FOR MVME133+BASE+E OFFSET
14  000000  2A7C 0000 0102 START:  MOVEA.L #STRTMSG,A5
15  000006  6100 00D0              BSR    MESSAGE
16                                 ********CHECK SECONDS 0-59 PARALLEL=FIFO TIME********
17  00000A  13C0 00FF 600D CHKSEC           MOVE.B  D0,IPFIFR     CLEAR FIFO OF IRQ0 TEST DATA
18  000010  6100 0076                      BSR    TAGNPAR        GET TIME TAG FIFO DATA & PARALLEL TIME
19  000014  207C 0000 00FA                 MOVEA.L #HISAV+8,A0
20  00001A  247C 0000 0102                 MOVEA.L #DELTA+8,A2
21  000020  023C 0000                      ANDI.B  #0,CCR
22  000024  323C 0007                      MOVE    #7,D1          DO 8 BYTES
23  000028  1520              DELTLOP      MOVE.B  -(A0),-(A2)    DELTA = PARALLEL - FIFO
24  00002A  4A1A                           TST.B   (A2)+          SBCD NEEDS AUTODEC MODE
25  00002C  8509                           SBCD    -(A1),-(A2)
26  00002E  51C9 FFF8                      DBF     D1,DELTLOP
27  000032  6100 0042                      BSR     WT100          LIMIT MAX EVENT RATE
28  000036  3239 0000 0100                 MOVE    DELTA+6,D1
29  00003C  0241 FFF0                      ANDI    #$FFF0,D1      ONLY DISPLAY IF BIG DELTA
30  000040  67C8                           BEQ     CHKSEC
31  000042  2A7C 0000 0141                 MOVEA.L #ASCBUF,A5     CONVERT FIFO, PAR, DELT TO ASCII
32  000048  323C 0017                      MOVE    #24-1,D1       LOOP COUNT FOR 24 BYTES
33  00004C  1E19              ASCLOP       MOVE.B  (A1)+,D7       GET 2 NIBBLES
34  00004E  3407                           MOVE    D7,D2          SAVE A COPY
35  000050  E84F                           LSR     #4,D7          RIGHT JUSTIFY HI ORDER NIBBLE
36  000052  0207 000F                      ANDI.B  #$0F,D7
37  000056  0607 0030                      ADDI.B  #"0",D7
38  00005A  1AC7                           MOVE.B  D7,(A5)+
39  00005C  0202 000F                      ANDI.B  #$0F,D2
40  000060  0602 0030                      ADDI.B  #"0",D2
41  000064  1AC2                           MOVE.B  D2,(A5)+
42  000066  51C9 FFE4                      DBF     D1,ASCLOP
43  00006A  2A7C 0000 0141                 MOVEA.L #ASCBUF,A5
44  000070  6100 0066                      BSR     MESSAGE
45  000074  6094                           BRA     CHKSEC
46  000076  303C 00FF              WT100:  MOVE    #$FF,D0
47  00007A  0839 0001 00FF 6001    WT100L: BTST.B  #1,IPSTS       LIMITS LOOP SPEED TO I/O SPEED
48  000082  51C8 FFF6                      DBF     D0,WT100L
49  000086  4E75                    WTRTS:  RTS
50                                 ******** SUBROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6 *****
51  000088  13FC 0000 00FF 6009    TAGNPAR MOVE.B  #0,IPTAG       TRIGGER EVENT BCD TIME REPORT
52  000090  33F9 00FF 6008 0000            MOVE    IPLO,HISAV+6
        00F8
53  00009A  33F9 00FF 600A 0000             MOVE    IPLO+2,HISAV+4
        00F6
54  0000A4  33F9 00FF 600C 0000             MOVE    IPLO+4,HISAV+2
        00F4
55  0000AE  33F9 00FF 600E 0000             MOVE    IPLO+6,HISAV
```

```
 56  0000B8   227C 0000 00E8                    MOVEA.L #EVTDAT-2,A1
 57  0000BE   323C 0009                         MOVE    #9,D1
 58  0000C2   0839 0000 00FF 6001     WTFIFA:  BTST.B  #0,IPSTS      READ 10 BYTES OF FIFO DATA
 59  0000CA   67F6                              BEQ     WTFIFA
 60  0000CC   12F9 00FF 6003                    MOVE.B  IPFIFO,(A1)+  READ WITHOUT MESSING UP A REGISTER
 61  0000D2   51C9 FFEE                         DBF     D1,WTFIFA
 62  0000D6   4E75                              RTS
 63  0000D8   3C4D                   MESSAGE:MOVE    A5,A6
 64  0000DA   4A1E                    MSGEND: TST.B   (A6)+        FIND END OF MESSAGE
 65  0000DC   66FC                              BNE     MSGEND
 66  0000DE   4A26                              TST.B   -(A6)
 67  0000E0   4E4F                              TRAP    #15
 68  0000E2   0002                              DW      $2
 69  0000E4   4E75                              RTS
 70  0000E6   0000 0000                         LWORD   0
 71  0000EA   0000 0000 0000 0000     EVTDAT: LWORD   0,0
 72  0000F2   0000 0000 0000 0000     HISAV:  LWORD   0,0   SEC,FRAC
 73  0000FA   0000 0000 0000 0000     DELTA:  LWORD   0,0
 74  000102   53 49 4D 20 45 58       STRTMSG:ASCII   SIM EXT EVT, READ PARALLEL, DISPLAY BIG DELTA PARALLEL-EXT EVT
 75  000140   00                              .BYTE   0
 76  000141   30 30 30 30 30 30       ASCBUF: ASCII   000000000000000000000000000000000000000000000000
 77  000171   00                              .BYTE   0
 78  000172                                    END


      Lines Assembled :  78          Assembly Errors :  0
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3                                       ********************************************************************************
 4                                      * TITLE IPTST3.001 7NOV94 JCK TPRO-IP VME BUS LATCHED VS LATCHED DELTA
 5                                      * NOTE: FOR THIS DEMO, HOST IS A XYCOM XVME-600 (10 MHZ 68000)
 6                                      ********************************************************************************
 7        00FF 6008                     IPLO    EQU     $FF6008         A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
 8  000000  2A7C 0000 00EA              START:  MOVEA.L #STRTMSG,A5
 9  000006  6100 00B8                          BSR     MESSAGE
10                                      ********CHECK SECONDS 0-59 PARALLEL=FIFO TIME********
11  00000A  33F9 00FF 6008 0000         CHKSEC  MOVE    IPLO,EVTDAT+6
12  000014  33F9 00FF 600A 0000                 MOVE    IPLO+2,EVTDAT+4
13  00001E  33F9 00FF 600C 0000                 MOVE    IPLO+4,EVTDAT+2
14  000028  33F9 00FF 600E 0000                 MOVE    IPLO+6,EVTDAT
15  000032  33F9 00FF 6008 0000                 MOVE    IPLO,HISAV+6
16  00003C  33F9 00FF 600A 0000                 MOVE    IPLO+2,HISAV+4
17  000046  33F9 00FF 600C 0000                 MOVE    IPLO+4,HISAV+2
18  000050  33F9 00FF 600E 0000                 MOVE    IPLO+6,HISAV
19  00005A  227C 0000 00DA                      MOVEA.L #EVTDAT+8,A1
20  000060  207C 0000 00E2                      MOVEA.L #HISAV+8,A0
21  000066  247C 0000 00EA                      MOVEA.L #DELTA+8,A2
22  00006C  023C 0000                           ANDI.B  #0,CCR
23  000070  323C 0007                           MOVE    #7,D1           DO 8 BYTES
24  000074  1520                    DELTLOP MOVE.B  -(A0),-(A2)     DELTA = PARALLEL - FIFO
25  000076  4A1A                                TST.B   (A2)+           SBCD NEEDS AUTODEC MODE
26  000078  8509                                SBCD    -(A1),-(A2)
27  00007A  51C9 FFF8                           DBF     D1,DELTLOP
28  00007E  3239 0000 00E8                      MOVE    DELTA+6,D1
29  000084  0241 FFC0                           ANDI    #$FFC0,D1       ONLY DISPLAY IF BIG DELTA
30  000088  6780                                BEQ     CHKSEC
31  00008A  2A7C 0000 0119                      MOVEA.L #ASCBUF,A5      CONVERT FIFO, PAR, DELT TO ASCII
32  000090  323C 0017                           MOVE    #24-1,D1        LOOP COUNT FOR 24 BYTES
33  000094  1E19                    ASCLOP  MOVE.B  (A1)+,D7        GET 2 NIBBLES
34  000096  3407                                MOVE    D7,D2           SAVE A COPY
35  000098  E84F                                LSR     #4,D7           RIGHT JUSTIFY HI ORDER NIBBLE
36  00009A  0207 000F                           ANDI.B  #$0F,D7
37  00009E  0607 0030                           ADDI.B  #"0",D7
38  0000A2  1AC7                                MOVE.B  D7,(A5)+
39  0000A4  0202 000F                           ANDI.B  #$0F,D2
40  0000A8  0602 0030                           ADDI.B  #"0",D2
41  0000AC  1AC2                                MOVE.B  D2,(A5)+
42  0000AE  51C9 FFE4                           DBF     D1,ASCLOP
43  0000B2  2A7C 0000 0119                      MOVEA.L #ASCBUF,A5
44  0000B8  6100 0006                           BSR     MESSAGE
45  0000BC  6000 FF4C                           BRA     CHKSEC
46  0000C0  3C4D                    MESSAGE:MOVE    A5,A6
47  0000C2  4A1E                     MSGEND: TST.B   (A6)+           FIND END OF MESSAGE
48  0000C4  66FC                             BNE     MSGEND
49  0000C6  4A26                             TST.B   -(A6)
50  0000C8  4E4F                             TRAP    #15
51  0000CA  0002                             DW      $2
52  0000CC  4E75                             RTS
53  0000CE  0000 0000                        LWORD   0
54  0000D2  0000 0000 0000 0000 EVTDAT: LWORD   0,0
55  0000DA  0000 0000 0000 0000   HISAV: LWORD   0,0   SEC,FRAC
56  0000E2  0000 0000 0000 0000   DELTA:  LWORD   0,0
57  0000EA  4D 45 41 53 55 52     STRTMSG:ASCII   MEASURE 2 PARALLEL TIMES, DISPLAY IF BIG DELTA
58  000118  00                               .BYTE   0
59  000119  30 30 30 30 30 30       ASCBUF: ASCII   00000000000000000000000000000000000000000000000000
60  000149  00                               .BYTE   0
```

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3                       ********************************************************************************
 4                              * TITLE IPTST4.001 7NOV94 JCK TPRO-IP VME BUS DISPLAY FIFO & PAR TIME & DELTA
 5                              * NOTE: FOR THIS DEMO, HOST IS A XYCOM XVME-600 (10 MHZ 68000)
 6                              ********************************************************************************
 7          00FF 6001           IPSTS     EQU    $FF6001
 8          0000 0000           BSTSOR    EQU    0           BIT0: FIFO NOT EMPTY    READ ONLY.
 9          00FF 6003           IPFIFO    EQU    $FF6003     FIFO DATA PORT (READ ONLY)
10          00FF 6009           IPTAG     EQU    $FF600D     FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
12          00FF 6008           IPLO      EQU    $FF6008     A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
13          00FF 600E           IPHI      EQU    $FF600E     A16 BUS WINDOW FOR MVME133+BASE+E OFFSET
14  000000  2A7C 0000 0106 START:    MOVEA.L #STRTMSG,A5
15  000006  6100 00D4              BSR     MESSAGE
16                              ********CHECK SECONDS 0-59 PARALLEL=FIFO TIME********
17  00000A  13C0 00FF 600DCHKSEC  MOVE.B  D0,IPFIFR     CLEAR FIFO OF IRQ0 TEST DATA
18  000010  6100 007A              BSR     TAGNPAR     GET TIME TAG FIFO DATA & PARALLEL TIME
19  000014  207C 0000 00FE         MOVEA.L #HISAV+8,A0
20  00001A  247C 0000 0106         MOVEA.L #DELTA+8,A2
21  000020  023C 0000              ANDI.B  #0,CCR
22  000024  323C 0007              MOVE    #7,D1       DO 8 BYTES
23  000028  1520           DELTLOP MOVE.B  -(A0),-(A2)  DELTA = PARALLEL - FIFO
24  00002A  4A1A                   TST.B   (A2)+       SBCD NEEDS AUTODEC MODE
25  00002C  8509                   SBCD    -(A1),-(A2)
26  00002E  51C9 FFF8              DBF     D1,DELTLOP
27  000032  6100 0046              BSR     WT100       LIMIT MAX EVENT RATE
28  000036  3239 0000 0104         MOVE    DELTA+6,D1
29  00003C  2A7C 0000 0145         MOVEA.L #ASCBUF,A5   CONVERT FIFO, PAR, DELT TO ASCII
30  000042  303C 0003              MOVE    #3,D0       DISPLAY FIFO, PAR, DELT
31  000046  323C 0007       ASCOLP  MOVE    #7,D1       LOOP COUNT FOR 8 BYTES
32  00004A  1E19            ASCLOP  MOVE.B  (A1)+,D7    GET 2 NIBBLES
33  00004C  3407                   MOVE    D7,D2       SAVE A COPY
34  00004E  E84F                   LSR     #4,D7       RIGHT JUSTIFY HI ORDER NIBBLE
35  000050  0207 000F              ANDI.B  #$0F,D7
36  000054  0607 0030              ADDI.B  #"0",D7
37  000058  1AC7                   MOVE.B  D7,(A5)+
38  00005A  0202 000F              ANDI.B  #$0F,D2
39  00005E  0602 0030              ADDI.B  #"0",D2
40  000062  1AC2                   MOVE.B  D2,(A5)+
41  000064  51C9 FFE4              DBF     D1,ASCLOP
42  000068  4A1D                   TST.B   (A5)+       LEAVE A SPACE
43  00006A  51C8 FFDA              DBF     D0,ASCOLP
44  00006E  2A7C 0000 0145         MOVEA.L #ASCBUF,A5
45  000074  6100 0066               BSR     MESSAGE
46  000078  6090                   BRA     CHKSEC
47  00007A  303C 00FF       WT100:  MOVE    #$FF,D0
48  00007E  0839 0001 00FF 6001     WT100L: BTST.B  #1,IPSTS     LIMITS LOOP SPEED TO I/O SPEED
49  000086  51C8 FFF6                   DBF     D0,WT100L
50  00008A  4E75            WTRTS:  RTS
51                              ******** SUBROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6 *****
52  00008C  13FC 0000 00FF 6009     TAGNPAR MOVE.B  #0,IPTAG     TRIGGER EVENT BCD TIME REPORT
53  000094  33F9 00FF 6008 0000     MOVE    IPLO,HISAV+6
            00FC
54  00009E  33F9 00FF 600A 0000     MOVE    IPLO+2,HISAV+4
            00FA
55  0000A8  33F9 00FF 600C 0000     MOVE    IPLO+4,HISAV+2
            00F8
56  0000B2  33F9 00FF 600E 0000     MOVE    IPLO+6,HISAV
```

```
                00F6
57  0000BC  227C 0000 00EC                  MOVEA.L #EVTDAT-2,A1
58  0000C2  323C 0009                       MOVE    #9,D1
59  0000C6  0839 0000 00FF 6001 WTFIFA:  BTST.B  #0,IPSTS     READ 10 BYTES OF FIFO DATA
60  0000CE  67F6                            BEQ     WTFIFA
61  0000D0  12F9 00FF 6003                  MOVE.B  IPFIFO,(A1)+  READ WITHOUT MESSING UP A REGISTER
62  0000D6  51C9 FFEE                       DBF     D1,WTFIFA
63  0000DA  4E75                            RTS
64  0000DC  3C4D                 MESSAGE:MOVE    A5,A6
65  0000DE  4A1E                  MSGEND: TST.B   (A6)+       FIND END OF MESSAGE
66  0000E0  66FC                            BNE     MSGEND
67  0000E2  4A26                            TST.B   -(A6)
68  0000E4  4E4F                            TRAP    #15
69  0000E6  0002                            DW      $2
70  0000E8  4E75                            RTS
71  0000EA  0000 0000                       LWORD   0
72  0000EE  0000 0000 0000 0000 EVTDAT:  LWORD   0,0
73  0000F6  0000 0000 0000 0000    HISAV:   LWORD   0,0   SEC,FRAC
74  0000FE  0000 0000 0000 0000    DELTA:   LWORD   0,0
75  000106  53 49 4D 20 45 58    STRTMSG:   ASCII   SIM EXT EVT, READ PARALLEL, DISPLAY BIG DELTA PARALLEL-EXT EVT
76  000144  00                              .BYTE   0
77  000145  30 30 30 30 30 30       ASCBUF: ASCII   0000000000000000 0000000000000000 0000000000000000
78  000177  00                              .BYTE   0
79  000178                                  END


    Lines Assembled :  79          Assembly Errors :  0
```

```
3                                       ********************************************************************************
4                                       * TITLE IPTST5.001 7NOV94 JCK TPRO-IP EXT EVT INTERRUPT TEST
5                                       * THIS DEMO ASSUMES A XYCOM XVME-600 (10 MHZ 68000) + GREENSPRING VIPC310
6                                       * THIS DEMO ASSUMES A XYCOM XVME-600 (10 MHZ 68000) + GREENSPRING VIPC310
7                                       ********************************************************************************
8         00FF 6001                     IPSTS           EQU   $FF6001
9         0000 0000                     BSTSOR          EQU   0          BIT0: FIFO NOT EMPTY    READ ONLY.
10        0000 0004                     BEXTENB         EQU   4          BIT6: EXTERNAL EVENT ENABLE. READ/WRITE
11        0000 0007                     BORIE           EQU   7          INTERRUPT ENABLE
12        00FF 6003                     IPFIFO          EQU   $FF6003    FIFO DATA PORT (READ ONLY)
13        00FF 6005                     IPVEC           EQU   $FF6005    INTR VECTOR FOR IRQ0 (READ/WRITE)
14        00FF 600D                     IPFIFR          EQU   $FF600D    FIFO RESET. ALSO CLEARS RESET. WRITE ONLY
15        00FF 6008                     IPLO            EQU   $FF6008    A16 BUS WINDOW FOR MVME133+BASE+8 OFFSET
16  000000  13C0 00FF 600D             START:          MOVE.B  D0,IPFIFR    CLEAR FIFO OF IRQ0 TEST DATA
17  000006  21FC 0000 00A2 0100                        MOVEA.L #INT0ISR,$100
18  00000E  13FC 0040 00FF 6005                        MOVE.B  #$40,IPVEC
19  000016  46FC 2000                                  MOVE    #$2000,SR    SET STS LEV = TO ALLOW INTR1
20  00001A  13FC 0090 00FF 6001                        MOVE.B  #1.SHL.BORIE+1.SHL.BEXTENB,IPSTS  ENABLE FIFO OR INTR
21  000022  0C39 0064 0000 0126     CHKSEC  CMPI.B  #100,EVTCNT  DISPLAY EVERY 100TH SET OF EXT EVT,PAR,DELTA
22  00002A  66F6                                       BNE     CHKSEC
23  00002C  13FC 0000 0000 0126                        MOVE.B  #0,EVTCNT    RESET COUNT
24  000034  207C 0000 011E                             MOVEA.L #HISAV+8,A0
25  00003A  227C 0000 0116                             MOVEA.L #EVTDAT+8,A1
26  000040  247C 0000 0126                             MOVEA.L #DELTA+8,A2
27  000046  023C 0000                                  ANDI.B  #0,CCR
28  00004A  323C 0007                                  MOVE    #7,D1        DO 8 BYTES
29  00004E  1520                            DELTLOP MOVE.B  -(A0),-(A2)  DELTA = PARALLEL - FIFO
30  000050  4A1A                                       TST.B   (A2)+        SBCD NEEDS AUTODEC MODE
31  000052  8509                                       SBCD    -(A1),-(A2)
32  000054  51C9 FFF8                                 DBF     D1,DELTLOP
33  000058  3239 0000 0124                            MOVE    DELTA+6,D1
34  00005E  2A7C 0000 0127                             MOVEA.L #ASCBUF,A5   CONVERT FIFO, PAR, DELT TO ASCII
35  000064  303C 0003                                  MOVE    #3,D0        DISPLAY FIFO, PAR, DELT
36  000068  323C 0007                       ASCOLP  MOVE    #7,D1        LOOP COUNT FOR 8 BYTES
37  00006C  1E19                            ASCLOP  MOVE.B  (A1)+,D7     GET 2 NIBBLES
38  00006E  3407                                       MOVE    D7,D2        SAVE A COPY
39  000070  E84F                                       LSR     #4,D7        RIGHT JUSTIFY HI ORDER NIBBLE
40  000072  0207 000F                                 ANDI.B  #$0F,D7
41  000076  0607 0030                                  ADDI.B  #"0",D7
42  00007A  1AC7                                       MOVE.B  D7,(A5)+
43  00007C  0202 000F                                  ANDI.B  #$0F,D2
44  000080  0602 0030                                  ADDI.B  #"0",D2
45  000084  1AC2                                       MOVE.B  D2,(A5)+
46  000086  51C9 FFE4                                 DBF     D1,ASCLOP
47  00008A  4A1D                                       TST.B   (A5)+        LEAVE A SPACE
48  00008C  51C8 FFDA                                 DBF     D0,ASCOLP    DISPLAY 3 16 DIGIT NUMBERS
49  000090  2A7C 0000 0127                             MOVEA.L #ASCBUF,A5
50  000096  2C7C 0000 0159                             MOVEA.L #ASCEND,A6
51  00009C  4E4F                                       TRAP    #15
52  00009E  0002                                       DW      $2
53  0000A0  6080                                       BRA     CHKSEC
54                          **INTERRUPT SERVICE ROUTINE TAGS TIME IN FIFO & READS PARALLEL INTO HISAV..HISAV+6 *****
55  0000A2  48E7 4040                       INT0ISR: MOVEM.L D1/A1,-(A7)
56  0000A6  13FC 0010 00FF 6001                        MOVE.B  #1.SHL.BEXTENB,IPSTS  DISABLE FIFO OR INTERRRUPTS WHILE READING FIFO
57  0000AE  0639 0001 0000 0126                        ADDI.B  #1,EVTCNT
58  0000B6  33F9 00FF 6008 0000             TAGNPAR MOVE    IPLO,HISAV+6
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59  0000C0   33F9 00FF 600A 0000                    MOVE    IPLO+2,HISAV+4
          011A
 60  0000CA   33F9 00FF 600C 0000                    MOVE    IPLO+4,HISAV+2
          0118
 61  0000D4   33F9 00FF 600E 0000                    MOVE    IPLO+6,HISAV
          0116
 62  0000DE   227C 0000 010C                         MOVEA.L #EVTDAT-2,A1
 63  0000E4   323C 0009                              MOVE    #9,D1       READ 10 BYTES OF FIFO DATA
 64  0000E8   0839 0000 00FF 6001            WTFIFA: BTST.B  #0,IPSTS    FOR EACH BYTE, CHECK FOR READY. **IMPORTANT!**
 65  0000F0   67F6                                   BEQ     WTFIFA
 66  0000F2   12F9 00FF 6003                         MOVE.B  IPFIFO,(A1)+  READ WITHOUT MESSING UP A REGISTER
 67  0000F8   51C9 FFEE                              DBF     D1,WTFIFA
 68  0000FC   13FC 0090 00FF 6001                    MOVE.B  #1.SHL.BORIE+1.SHL.BEXTENB,IPSTS  REENABLE FIFO NOT EMPTY INTR
 69  000104   4CDF 0202                      EVTISR  MOVEM.L (A7)+,D1/A1    RESTORE A0 AND D0
 70  000108   4E73                                   RTE
 71  00010A   0000 0000                      LWORD   0
 72  00010E   0000 0000 0000 0000    EVTDAT: LWORD   0,0
 73  000116   0000 0000 0000 0000    HISAV:  LWORD   0,0   SEC,FRAC
 74  00011E   0000 0000 0000 0000    DELTA:  LWORD   0,0
 75  000126   00                      EVTCNT: .BYTE   0
 76  000127   30 30 30 30 30 30      ASCBUF: ASCII   0000000000000000 0000000000000000 0000000000000000
 77  000159   00                      ASCEND:.BYTE    0
 78  00015A                                   END


      Lines Assembled :  78          Assembly Errors :  0
```

10 Driver Support

Please contact your sales representative for information about Spectracom's bus-level timing board driver support for a variety of other platforms. You may also visit our website at www.spectracomcorp.com to download datasheets and manuals.

REVISION HISTORY

Revision Level	***ECN Number***	***Description***
A	**2187**	First conversion of legacy KSI documentation (level 4.1).

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